Design & Simulation Of 3-Phase, 19-Level Inverter few number of components for industrial applications

[1]Ravi Naragani
[1]Assistant Professor, [1]Department of Electrical and Electronics Engineering, HITAM, Hyderabad, India

Abstract: This paper deals with study of three phases Nineteen Level inverter fed induction motor drive. The nineteen levels are realized by cascading Two H- Bridges. The poor quality of voltage and current of a conventional inverter fed induction machine is due to the presence of harmonics and hence there is significant level of energy losses. The Multilevel inverter is used to reduce the harmonics. The inverters with a large number of steps can generate high quality voltage waveforms. The higher levels can follow a voltage reference with accuracy and with the advantage that the generated voltage can be modulated in amplitude instead of pulse-width modulation. The CHB topology consists of several H- bridges and dc sources. This topology is implemented to three-phase system. In the symmetric structure, the values of the dc voltage sources are same. However, in asymmetric topology the magnitudes of the dc voltage sources are unequal. Asymmetric CHB topology generates a large number of levels for the same number of components in comparison with symmetric topology for the same number of power electronic components. For asymmetric inverters, a new structure has been recommended in, which reduces the number of switches and dc voltage sources compared with the CHB inverter. However, for creating a large number of output. Multilevel inverters with more number of levels can produce high quality voltage waveforms. In this concept three-phase is used instead of single-phase and implemented for nineteen levels, which can generate a large number of levels with reduced number of IGBTs, gate driver circuits and diodes. A comparison is presented between proposed multilevel inverter and conventional cascade topology.

IndexTerms: Induction motor, Matlab/simulink, Multilevel inverters, voltage source invert and, Total Harmonic distortion

I.INTRODUCTION

Advancement in the research of Power electronic inverters is still increasing with the rapid demands in electrical systems. The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum [10].

Multilevel converters are mainly utilized to synthesis a desired single- or three-phase voltage waveform. The desired multi-staircase output voltage is obtained by combining several dc voltage sources. Solar cells, fuel cells, batteries and ultra-capacitors are the most common independent sources used [1]. One important application of multilevel converters is focused on medium and high-power conversion. Nowadays, there exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs)[2]. Among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology [3].

Diode-clamped multilevel converters are used in conventional high-power ac motor drive applications like conveyors, pumps, fans, and mills. They are also been applied where high power and power quality are essential, for example, static synchronous compensators active filter and reactive power compensation applications, photovoltaic power conversion, uninterruptible power supplies, and magnetic resonance imaging. Furthermore, one of the growing applications for multilevel motor drives is electric and hybrid power trains.

For increasing voltage levels the number of switches also will increase in number. Hence the voltage stresses and switching losses will increase and the circuit will become complex. By using the proposed topology number of switches will reduce significantly and hence the efficiency will improve.

A multi-stage inverter using three-state converters is being analyzed for multipurpose applications, such as active power filters, static var compensators and machine drives for sinusoidal and trapezoidal current applications. The great advantage of this kind of converter is the minimum harmonic distortion obtained.

The circuit of Fig.1 shows the basic topology of one converter used for the implementation of multi- stage converters. It is based on the simple, four switches converter, used for single phase inverters or for dual converters. These converters are able to produce three levels of voltage in the load: +Vdc, - Vdc, and Zero [7].

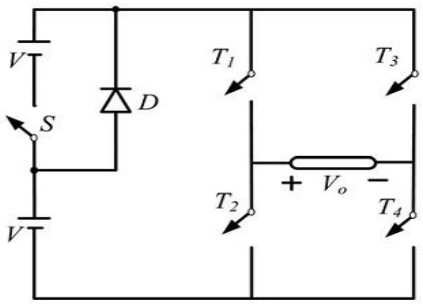


Fig.1. Basic idea diagram module for building multi stage inverter

This paper mainly focuses on the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels. Here , in this paper the proposed multilevel scheme extended up to 19- levels.. In this work, the asymmetric 19 level inverter is presented. This inverter is designed to avoid the regeneration problem - power flow from the load to the inverter - in some of the power cells. This is achieved by obtaining the firing angles associated with the power cells considering a minimum load voltage THD. The simulation and experimental results of the proposed 19-level inverter topology are also presented. Finally, a power flow analysis is accomplished and simulated results show the feasibility of this approach

II.PROPOSED19-LEVEL INVERTER

Multilevel inverters are the alternative for medium voltage applications. Within the inverters types there are symmetric and asymmetric topologies. The asymmetric inverters have different DC voltage values. The most common topology is when the different cells are implemented in cascade arrangement, where the DC voltage are in multiples of 3, obtaining an AC voltage with $3^n = 27$ levels (n = 3 cascaded inverters). This topology provides a load voltage with low harmonic content, THD <; 3%. However, this high quality voltage has a non-negligible drawback, which is the presence of regeneration in some of the inverters, independent of load type [1]. This phenomenon is due to the modulation technique (Nearest Level Modulation) used by this inverter. In this work, the asymmetric 19 level inverter is presented. This inverter is designed to avoid the regeneration problem - power flow from the load to the inverter - in some of the power cells. This is achieved by obtaining the firing angles associated with the power cells considering a minimum load voltage THD. Finally, a power flow analysis is accomplished and simulated results show the feasibility of this approach.
Fig.2 shows the proposed inverter fed to 3-phase a.c load and Fig.3 shows the simplified diagram with three inverters per phase.

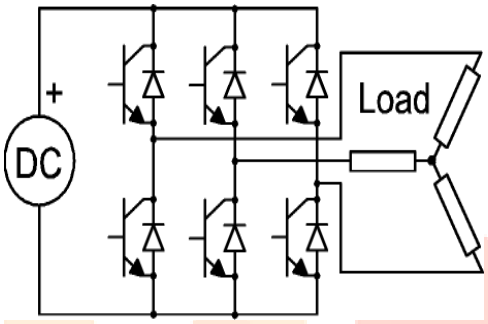


Fig.2. Basic idea diagram of three-phase inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage.

A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors,C1 andC2. The voltage stress across each switching device is limited to Vdc through the clamping diodes Dc1 andDc2. It is assumed that the total dc link voltage is Vdcand mid point is regulated at half of the dc link voltage, the voltage across each capacitor isVdc/2(Vc1=Vc2=Vdc/2).[1]

Table 1 ON switches look-up table for basic circuit of the proposed multilevel inverter

State	Switches states					Output voltage
	S	T_1	T_2	T_3	T_4	
1	0	1	0	1	0	0
2	0	1	0	0	1	V
3	0	0	1	1	0	$-V$
4	1	1	0	0	1	$2V$
5	1	0	1	1	0	$-2V$

A. Switching Sequences:

In order to avoid unwanted voltage levels during switching cycles, the switching modes should be selected so that the switching transitions become minimal during each mode transfer. This will also help to decrease switching power dissipation In order to produce 19- levels by Sinusoidal Pulse Width Modulation (SPWM), three saw- tooth waveforms for carrier and a sinusoida reference signal for modulator are required as shown in Fig. 4.

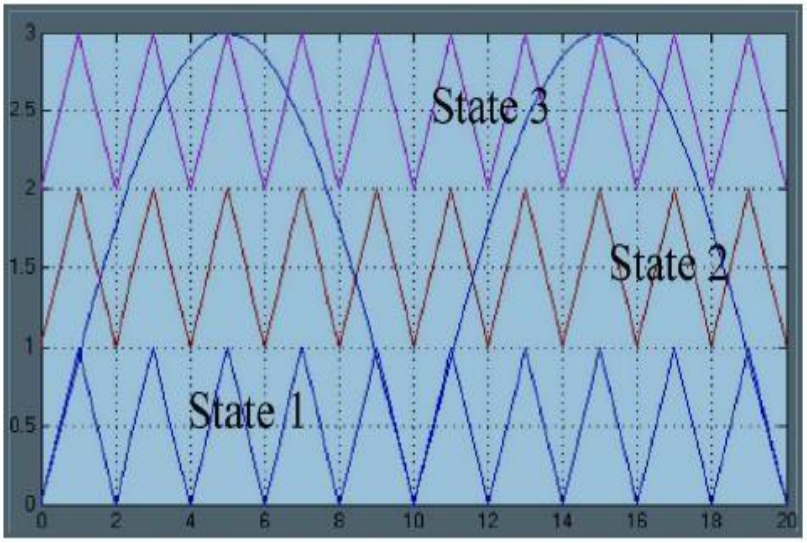
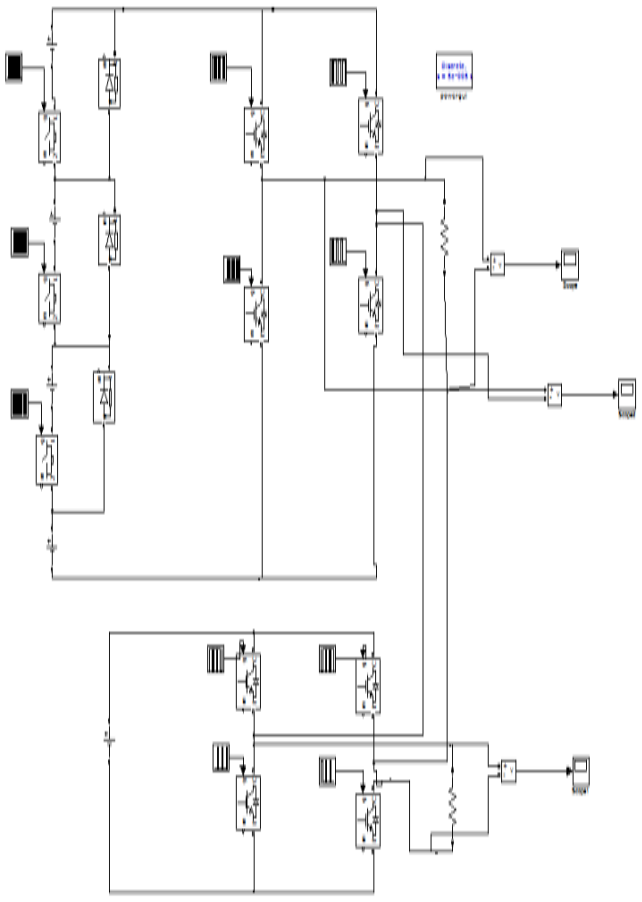


Fig. 4.SPWM carrier and modulator for proposed 19- level inverter

III MATLAB BASED SIMULATION& RESULTS

A. MATLAB based simulation:

Fig.5. shows the complete MATLAB based simulation masked diagram of the proposed 19-level, 3-phase inverter.



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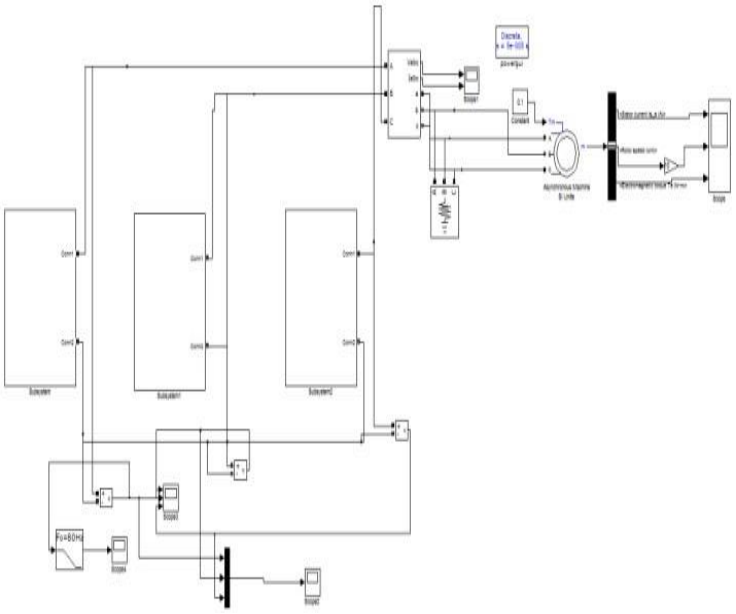

Fig.6. Nineteen-Level Based MLI with Induction Motor

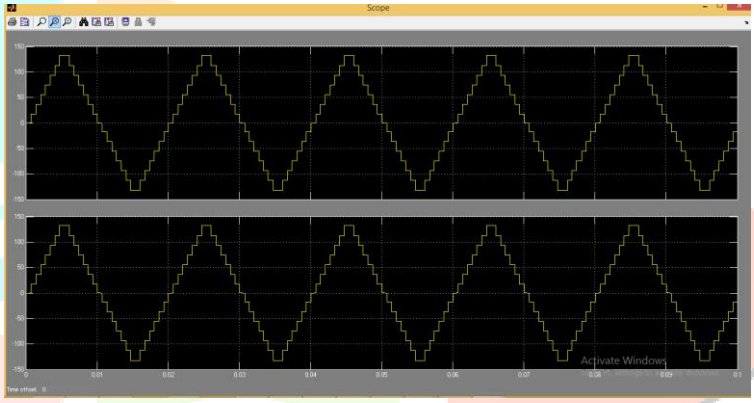

Fig.7. output voltage of three phase nineteen level inverter

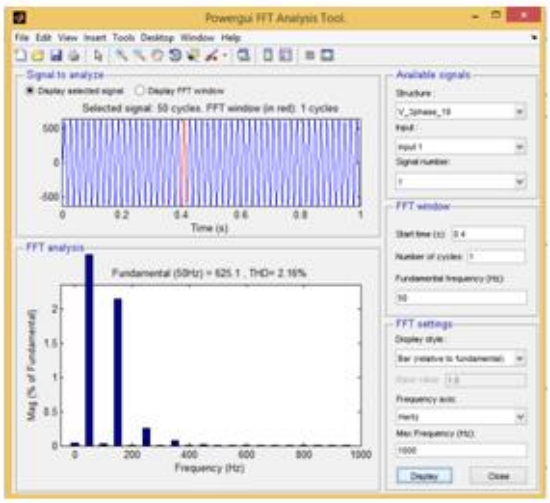

Fig.8. FFT analysis and THD value

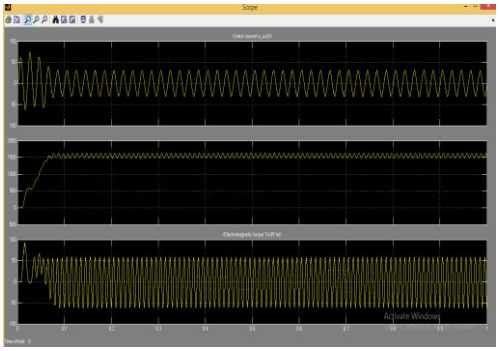

Fig.9.Current, Speed and Torque for Induction Motor.

Fig.12 Output voltages three phase nineteen level inverter.

TABLE1.SIMULATION SPECIFICATIONS

Parameter	*Rating*
Input DC supply (V)	50V
IGBT/Diode Internal Resistance Ron	1 m Ω
Snubber Resistance , Rs (Ω)	1μΩ
Nominal frequency (Hz)	50 Hz
Active Power (W)	10KW
Reactive Power (Var)	8Kvar
Damping factor of filter	0.8

IV.CONCLUSION

An efficient 3-phase, 19-level inverter is presented in the paper. The resultant simulation graphs show the accuracy of the proposed inverter. High performance switches are adopted to reduce the conduction losses and improve the efficiency. Experimental results that confirm the feasibility of the proposed 3-phase, 19-level inverter. Finally, MATLAB based simulink results shown the THD value at reasonable level.

V.REFERENCES

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Author Details:

Mr. N. Ravi working as an Assistant Professor in Dept. of EEE in Hyderabad institute of technology & Management. He is having10 years of teaching experience. He did his B. Tech from AGCET college of Engineering and Technology, JNTUK and he is completed M. Tech in Power Electronics from AGCET college of engineering and Technology. His area of interest is Power Electronics and electrical machines.