IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Comparative Analysis of MUX Using Various CMOS Circuit Style under Nanometer Technology

Ekansh Agarwaal
ABES Eng. College

Divyanshu Maheshwari
ABES Eng. College

Lakshya Goel
ABES Eng. College

Jitendra Saraswat
ABES Eng. College

***Abstract*—This paper explains the designs of various CMOS circuit families including Static CMOS circuit, Pseudo NMOS circuit, Domino logic circuit and Dual-Rail Domino logic circuit by using VLSI software: LT Spice XVII with layout tools at 45 nm, 90 nm and 180nm technology node. The working of these circuits is done through VLSI due to its high noise immunity and low static power. This gives us the comparative studies between various circuits and further calculated their delays, average energy. We will calculate the Total power dissipated using Static Power and Dynamic Power. Power Delay Product and Propagation Delay is further measured.**

Keywords: Static CMOS, Dynamic CMOS, Domino Logic CMOS, Dual-Rail Domino Logic CMOS, Average Power, Power Delay Product(PDP), Delay, Area

I. INTRODUCTION

A multiplexer is a device that takes one of many analog or digital input signals and transfers the selected input information into a single output line. The select lines determine which input is connected to the output, and also increase the amount of information that can be sent over a network within certain time. Its is also called a data selector. They are used to increase the amount of information that can be sent over a network within a determined value of frequency. The input lines as D_0 and D_1 with a select line S and an output line Y is taken for MUX design. The truth table is shown below table 1;

The logic output function is:

$$Y = \overline{S} \cdot D0 + S \cdot D1$$

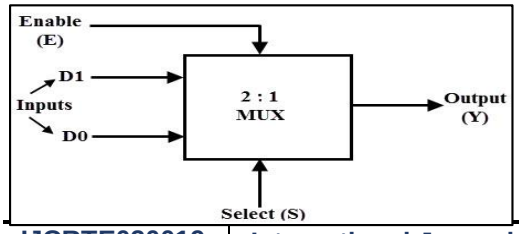

Fig 1-Structure of 2:1 MUX

TABLE I. TRUTH TABLE OF 2:1 MUX

SELECT LINE	INPUT		OUTPUT
~S/S	D1	D0	Y
1/0	X	0	0
1/0	X	1	1
0/1	0	X	0
0/1	1	X	1

On studying several journals and articles on our topic through CMOS VLSI Design: A Circuits and System Perspective, Design of multiplexer in multiple logic styles for low power VLSI" International Journal of Computer Trends and Technology and Design of Power efficient MUX using dual gate FinFET technology," IEEE Conference, 2016. We gather information about the best circuit that is to be used among Static, Dynamic, Domino logic, Dual-Rail Domino logic to give us minimum Power Delay.

The various types of CMOS Logic families on which we will perform our design will be:

- Static CMOS
- Dynamic CMOS
- Domino Logic CMOS
- Dual Rail Domino Logic

2.1 Static CMOS:

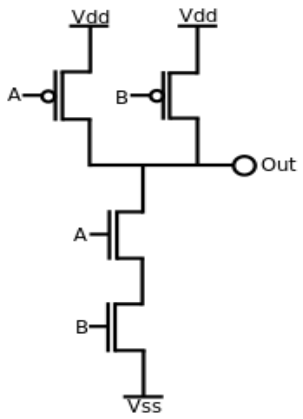

Fig 2: Structure of Static CMOS

Static CMOS is a circuit gates are implemented by building the two switch networks i.e. Pull up network (PUN) and Pull down network (PDN). In this circuit, NMOS has k inputs i.e. k number of NMOS and k inputs for PMOS also. Due to PMOS, overall size of this circuit is more. Due to PMOS, capacitive loading will be more.

Due to the large size of PMOS and slower switching capability, power dissipation will be more.

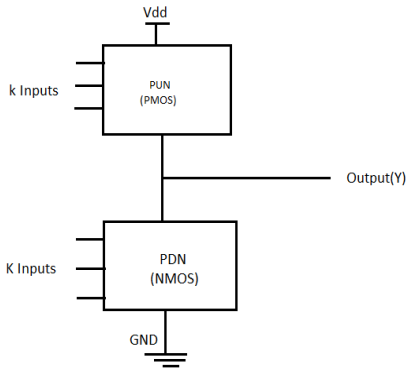

Fig 3- CMOS Static Logic

Basic features of Static CMOS logic are:

- No cascading issues
- Noise margins are relatively high
- Output impedance is low and input impedance is high
- The path between Vdd and ground is steady and zero

2.1.1 Designing 2:1 MUX using Static CMOS

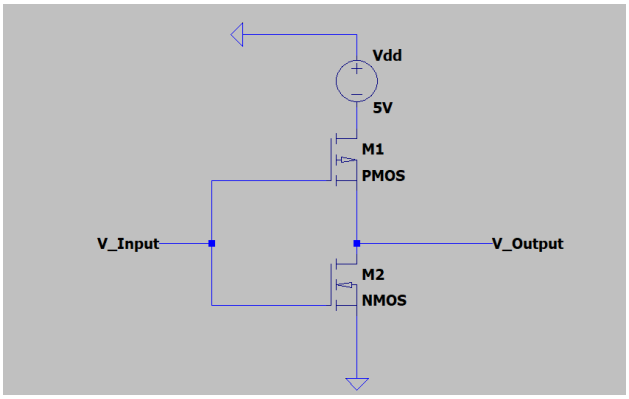

Fig 4- 2:1 MUX using Static CMOS

For construction of the PUN and PDN circuits, the observations that we can conclude are:

• A gate signal is given to CMOS logic due to which the

nMOS and pMOS behaves as a switch controlling device. When the gate signal (controlled) is high then an nMOS switch gives output as1 i.e. ON and is 0 i.e. OFF when the gate signal (controlled) is low. An inverse switch is generated by the pMOS device in which it is on due to the low voltage signal and off due to the high voltage signal.

• The construction of PDN is done using nMOSdevices, while for PUN circuits pMOS devices are used. The main reason for this construction is that nMOS devices makes the ground to pass through output and pMOS devices allows passing Vdd.

A major advantage of static design is that they have very low power dissipation, where either PUN or PDN is off for any given input signal. The major drawback with this kind of circuit is that larger cross-sectional area is needed for implementation.

2.1.2 Problems associated with Static Circuits:

The number of transistors required are 2N which is quite large.

The static Power loss is more.

It shows slower switching capability because of no load capacitance between Vdd and output.

2.1.3 Solution for this circuit:

Hence, we shift our analysis to a better circuit than static circuits which are Dynamic logic circuits.

2.2 Dynamic Circuit:

Dynamic logic is a transient circuit which is done with charging and selectively discharging of the capacitance. Static circuits maintain its output level throughout as long as power is applied to it. It depends on the temporary accumulation of electrons and holes in the parasitic capacitance of the node.

Silicon area for the dynamic circuits is made small which give better performance than conventional ones. Thus they are used widely in many areas. It also uses the Precharge and Evaluation processes that control the charging and discharging by the clock depending on input gates.

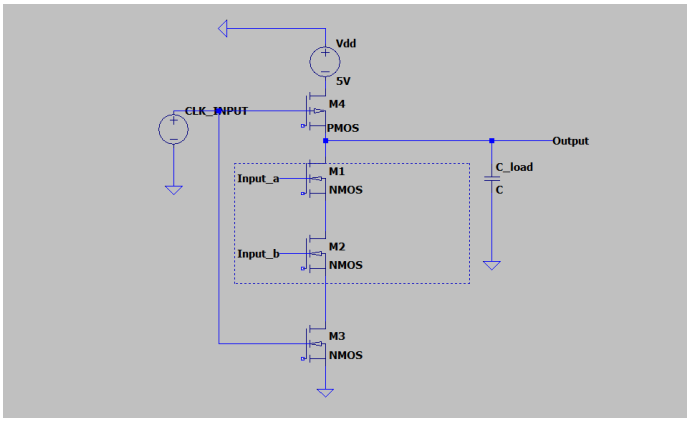

Fig 4- Structure of Dynamic CMOS

2.2.1 Designing 2:1 MUX using Dynamic CMOS logic

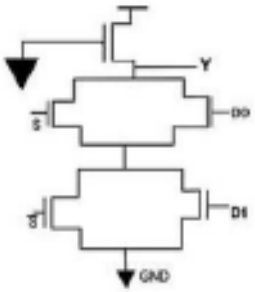

Fig 5- 2:1 MUX using Dynamic CMOS

Precharge Phase(clock to charge the capacitance):

It is the first phase When CLK = 0, the output node is driven at a very high rate to output voltage when precharge transistor is open. During that phase, evaluation transistor at the bottom is turned off so it is impossible to be driven low in this phase. The period. The power that is consumed statically during the precharged period is removed at the FET evaluation.

Evaluation phase (clock to discharge the capacitance counting on the condition of logic inputs):

It is the second phase When Φ = 1, the nMOS below PDN is turned on and the nMOS attached to VDD is turned off. Depending on the values on the inputs, output is bring down to zero. If not then the precharge state will remain at output capacitance.

So we can say that these two logic circuits possess distinct logic families. Static CMOS logic which are decided from static circuits and domino ones and pseudo NMOS logics which are decided from Dual Rail logic and dynamic circuits for the working of MUX.

2.3 **Domino logic:**

Domino Logic circuits solves the problem of cascading in Dynamic CMOS logic by adding Static CMOS inverter stage.

The addition of inverter allows us to operate a number of such structures in cascade. Reducing the number of transistors at the same time keeps a check on the static Power consumption.

The problem of monotonicity is removed by making first block of logic implemented in domino while the other one is built with static CMOS gates. The result goes to a latch after end of

the half cycle, and domino logic may resume at the beginning of next half-cycle.

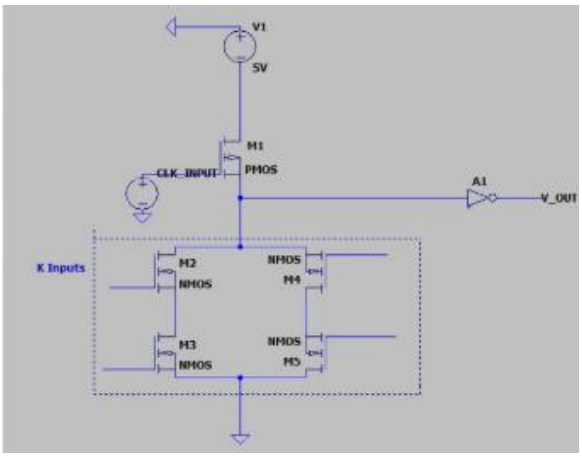

Fig 6- Domino Logic

3.1 Designing 2:1 MUX using Domino Logic:

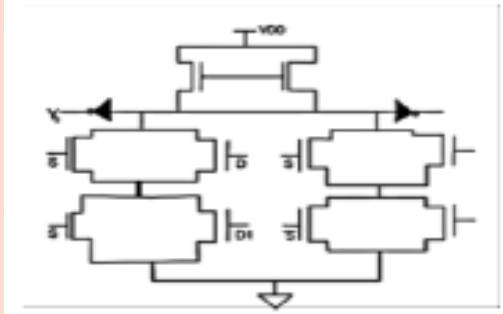

Fig 7- 2:1 MUX using Domino Logic

Operation of this circuit can be explained in two ways:

Precharge Mode: When clock(CLK) =0, The output node of Dynamic CMOS is at logic high and output of inverter becomes low. TheStatic power consumption between supply and ground will be zero.

Evaluation Mode: When CLK=1, at its beginning phase of evaluation, there are two possibilities:

- The output node of dynamic CMOS either discharged or remains high.
- Similarly, the inverter output voltage can also make transition from 0 to 1.

2.3.1 Problems associated with Domino CMOS Logic:

The drawback is that the inverting logic (static) should be an even multiple even so that next buffer stage shows transition from 0 to 1 transitions during evaluation phase.

The other limitations associated are the charge leakage between output nodes of dynamic and intermediate nodes of PDN logic block during when CLK=1 may give wrong output and signal information.

2.3.2 Solution and Improvement in the Circuit:

One possible solution to eliminate the problem is to feature weak pull up device(PMOS) with small (W/L) ratio which forces a high output level is one of the possible measures to avoid the output signals based on wrong information.

The weak PMOS will turned on during precharge, otherwise it will be turned off as Vout becomes high.

2.4 Dual-Rail Domino:

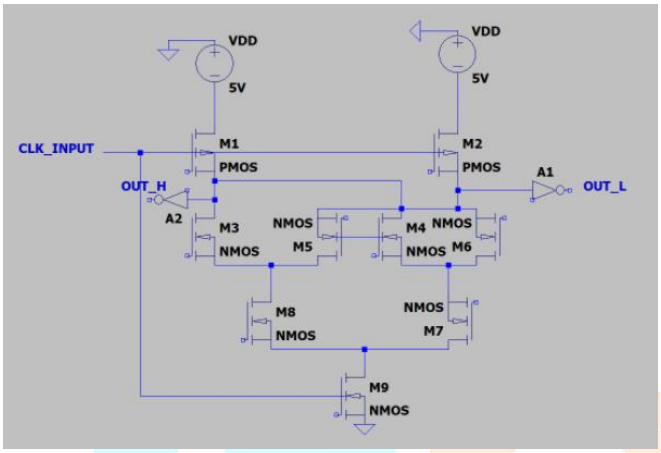

Fig 8- Structure of Dual-Rail Domino Logic

So far we working with single rails. In dual rail, we have:

- Non-inverted and inverted components exist simultaneously.
- It works on difference.
- Provides increased switching speed.

However, the complementing factor is increasing complexity and area overhead.

It is also called as Differential Cascade Voltage Switch Logic. These circuits possess latching characteristics

The first and second discharge areas, respectively connected to the same first and second members. The first and second static states each have a separate input location connected separately from the first and second nodes, respectively and each has a different output.

Each pre-charge and second pre-charge transistor are individually connected to obtain a single clock sequence of consecutive pre-charge and test phases, individually connected to output the first and second output nodes, respectively.

2.4.1 Designing 2:1 Multiplexer using Domino(Dual-Rail) Logic:

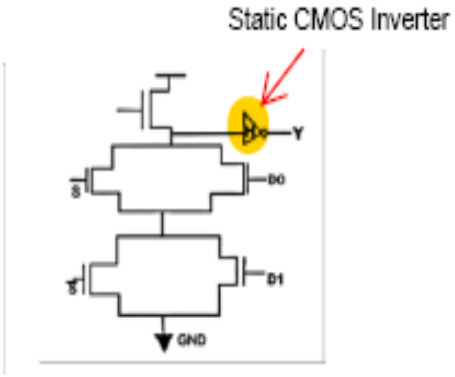

Fig 9- 2:1 MUX using Dual-Rail Domino Logic

Dual rail domino CMOS logic arises in the construction of domino CMOS circuits. Firstly, you must already be knowing that domino CMOS logic is used in order to avoid the clock skew problem where (in multi-stage CMOS circuits), if the clock for stage i+1 arrives earlier than the clock for stage i , stage i+1 is in evaluation whereas stage i is still in pre-charge. The "pre-charged" output of stage i when fed to the gate terminal of the NMOS transistors used in stage i+1 turns the aforementioned NMOS transistors ON and thus the output of the NMOS Block discharges and remains permanently at logic low, thus preventing the NMOS block from simulating the required functionality.

III. Technology and Performance Metrics Used

3.1 Working Tool for Simulation:

The whole work is implemented over a simulation tool CADANCE Virtuoso, this tool is assisted by variety of UNIX and PC based systems. It is used over 90nm and 180nm at an operating frequency of 2.8 GHz.

3.2 Evaluation based on Performance Matrices:

The experiments and observations are done to compare the different performance metrics for the optimal design of the MUX. Some of them are:

Power(Average) and Propagation Delay.

Components to find out the consumption of power in Complimentary MOS circuits are:

• Static Power

• Dynamic Power

3.2.1 Power Dissipation (Average): It is characterized as the aggregation of the Power(static) and the Power(dynamic). When input POWER is reduced then power dissipation or consumption will also get reduced.

The Unit of average power is Watt.

Average Power= Power(STATIC) + Power(DYNAMIC)

3.2.1.1 Dynamic Power:

Dynamic Dissipation is due to:

- "Short-circuit current" while both PMOS and NMOS stacks are partially ON.
- Charging and discharging load capacitances as gate switches.

3.2.1.2 Static Power:

It is due to the following reasons:

- Contention Current in ratioed circuits
- Gate Leakage through gate dielectric
- Sub-Threshold leakage through off transistors.
- Junction Leakage from source/drain diffusions.

$P_{dynamic} = P_{switching} + P_{short\text{-}circuit}$

$P_{static} = (I_{sub}+I_{gate}+I_{jun}+I_{cont})V_{dd}$

$P_{total} = P_{static} + P_{dynamic}$

3.2.2 Propagation Delay: It is explained as the interval of time required for input signal to be propagated to the output switches. It is the transitioning of the input-output signal when it reaches 50% of its final value and vice-versa.

Unit of Propagation delay-**Seconds (s).**

$$\textbf{Delay}=\frac{\{T(rf)+T(fr)\}}{2}$$

Where, $T(rf)$- RISE TIME$T(fr)$ – FALL TIME

3.2.3 Area: It is the multiplication of the length and breadth (dimensions of MUX taken) multiplied with total no. of transistors necessary to perform the implementation of the logical circuits.

Unit of the area is **sq. meter(m^2).**

Area=L*W*(No. of Transistors Required)

Where L is length, B is breadth and N is no. of transistors required.

3.2.4 Power delay product (PDP) is given by the multiplication of power(average) dissipation & propagation delay of circuit.

Unit of Power delay product is **joules(J).**

PDP=Average Power*Delay

Table 2: Performance Analysis of 2:1 MUX using various CMOS Logic Families

Name of Logic	Number of Transistors	Average Power	Delay	Area
Static CMOS	K PMOS K NMOS	Low	High	Large
Dynamic CMOS	K+1 NMOS 1 PMOS	High	Less than Static	Small
Domino Logic	K+1 NMOS 1 PMOS	Low	Lowest	Small
Dual-Rail Domino Logic	K+1 PMOS K+1 NMOS	Medium	Less than Static and Dynamic	Large

Performance Metrics for different logic Families(CMOS) is been demonstrated Therefore, inspection of performance parameter demonstrate the gross robustness of MUX(2:1) is built by make use of logic of domino for maximum efficiency.

IV. Conclusion:

Inside it, MUX(2:1) is studied by make use of different logic families of CMOS and performance metrics were analysed through various papers. It is examined that, CMOS NMOS domino MUX (2:1) planned by domino logic. This layout works very well for scale reduction and power utilization to the wide range of various logic families or PD(Delay) is moreover less, still in between at that place is compromise amid logic(domino) and static Complimentary MOS The CMOS concept is ignored when considered overall performance .so through general analysis it demonstrates that Power and latency of an effective AVERAGE POWER multiplexer can be built utilizing the domino concept that makes other logic families. Implication of Multiplexer to be used is similar within side by side (parallel) to series converter (one a significant use in Multiplexer) to lessen broad equal buses into sequential message (signal) within area of Telecommunications fields, Material (information) connection and Defence practises. Subsequently, in light of all the execution examination made in this work it is demonstrated that multiplexer designed to use Domino logic can be used in different applications to get better execution.

V. Acknowledgement:

We want to stretch out our gratitude to ABES Engineering College, Ghaziabad, who manage us with the Cadence Virtuoso tool on which we worked at 180 nm, 90 nm and 45 nm. We would also like to thank our mentors (**Ms. Pallavie Tyagi** and **Mr. Dheeraj Singh**) for guiding us throughout this project and giving us the golden opportunity to do this wonderful project.

REFERENCES:

[1] Neil H. E. Weste and David Money Harris, "CMOS VLSI Design A Circuits and System Perspective", Pearson Education (Asia) Pvt. Ltd.2000.

[2] J. M. Rabaey, A. Chandrakasan, and B. Nicolic, Digital Integrated Circuits: A Design Perspective, 2nd ed. Upper Saddle River, NJ: Prentice-Hall, 2003

[3] M. Padmaja, V.N.V. Satya Prakash, "Design of multiplexer in multiple logic styles for low power VLSI", International Journal of Computer Trends and Technology – volume 3 Issue 3 – 2012.

[4] Gurjeet Kaur, Gurmohan Singh, "Analysis of low power CMOS current comparison domino logic circuits in ultra deep submicron technologies," International Journal of Computer Applications (0975 – 8887), February 2014, Volume 88 – No.7.

[5] PurnimaKumari Sharma, Neeraj Kumar Singh, "Power comparison of single and dual rail 2:1 MUX design at different levels of technology," IEEE Conference, 2014, pp. 671-775.

[6] S. Abirami, M. Arul Kumar, E.Abinaya, J.Sowmaya, "Design and analysis of 2:1 multiplexer circuit for high performance,"

International Journal of Electrical and Electronics Engineers, Vol. No. 7, Issue No. 01, Jan-June, 2015

[7] PritiGupta , Rajesh Mehra, "Layout design and simulation of CMOS multiplexer," International Journal of Scientific Research Engineering &Technology(IJSRET),14-15 March,2015

[8] Mohit Vyas, SoumyaKanti Manna, ShyamAkashe, "Design of Power efficient MUX using dual gate FinFET technology," IEEE Conference, 2016.

[9] Ila Gupta, Nehra Arora, Prof.B.P.Singh, "Simulation and analysis of 2:1 multiplexer circuits at 90nm technology", International Journal of Modern Engineering Research (IJMER) – volume 1 Issue.2, pp-642-646.

[10] S. Vijayakumar and B. Karthikeyan, "Mixed style of Low Power Multiplexer Design for Arithmetic Architectures using 90nm Technology", *Proceedings of the 12th international conference on Networking VLSI and signal processing (ICNVS)*, pp. 83-87, February 2010.

[11] Pragati Gupta, Keshav Mehrotra, Khushboo Kashyap, Harmeet Kaur, Parth Dhall, "Area Efficient, Low Power 4:1 Multiplexer using NMOS 45nm Technology", International Journal on recent and innovation tr en ds in co mp u tin g and Computation, vol.4, no.4, pp.570- 574, April 2016.

[12] Chung-Yu Wu; Kuo-Hsing Cheng; Jinn-Shyan Wan. "Analysis and design of a new race-free four-phase CMOS logic", Solid-State Circuits, IEEE Journal of Volume 28, Issue 1, Jan 1993, pages 18-25.

[13] Purnima Kumari Sharma, Neeraj Kumar Singh, "Power comparison of single and dual rail 2:1 MUX design at different levels of technology," IEEE Conference, 2014, pp. 671-775.

[14] Pretorius JA, Shubat AS, Salama CAT. Charge redistribution and noise margins in domino CMOS logic. IEEE Transaction on Circuits System. 1986 Aug; 33(8):786–93.

[15] Wang L, Shanbhag NR. Noise-tolerant dynamic circuit design. Proceedings of International Symposium on Circuits Systems; 1999. p. 549–52