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DESIGN OF 32-BIT ADDER USING CARRY LOOK AHEAD ADDER

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Abstract: **Adders are an essentially universal component of today's integrated circuits. The constantly developing computing industry demands not just faster arithmetic units, but also smaller and less power consumption arithmetic circuits. The adder must be quick and also efficient in chip area to meet its requirements. In order to construct an adder of 32-bit using eight 4-bit adder for our project, we used the Carry look ahead adder. It is also known as fast adders because it consumes less time over other adders by propagating carry before the sum output is obtained, resulting in brilliant performance. We designed the schematic and layout of CLA using LT spice simulation programmed in Electric binary using 45nm technology.**

Index Terms **- Adder, CMOS, Electric, CLA.**

I. INTRODUCTION

Addition is the basic building block for numerous processing operations in electronics, including Arithmetic Logic Units, addresser, multiplier, and so on. The addition of a given number of bits to a digital circuit is a common operation used to reduce the complexity of the circuit and its operation. A onebit full adder design is created and simulated for transient simulation. The carry look ahead adder is a combination of ripple carry adder and carry look ahead logic unit. The carry look ahead adder (CLA) is analogous to the carry-skip adder in that it assesses both Carry generate and carry propagate signals to see if the first group creates a carry instead of waiting for a ripple from the previous adder.

In [1], the addition of a given number of bits is basic operation to reduce the difficulty of the circuits. All the types of 4-bit adders are compared that have been designed, simulated and verified using the Xilinx synthesis tool.

In [2], the adiabatic logic behind 16-bit adder using carry look ahead adder is explained. Also, it reduces the power consumption during the propagation and computation.

In [3], a 1-bit full adder cell is proposed which is less power consuming and high performance. For the simultaneous creation of XOR and XNOR functions, the Gate Diffusion Input (GDI) technique was applied.

In [4], explains that these the large family of addition structures as it shares minimum logical depth. It is possible to obtain accurate results both in area and low power/cost than other cases, as its transitional structure shows the tradeoffs amongstthe amount of internal wiring and the fanout of intermediate nodes.

If the implementation was using ripple carry adder, it faces the propagation delay problem. In some technique there is more difficulties in the circuits as well as in the operation. So, we have implemented Carry look ahead adder to overcome from these problems which is having less propagation delay.

II. CARRY LOOK AHEAD ADDER

A. 4- bit Carry look ahead adder

Carry lookahead adders depends on two terms, Carry Propagate and Carry Generate, which are denoted by C_p and C_g. The propagate bit is passed on to the next stage, and the generate bit is utilized to generate the carry out bit, which is distinct to the input carry bit. The 4-bit carry look ahead adder architecture is shown Fig1:

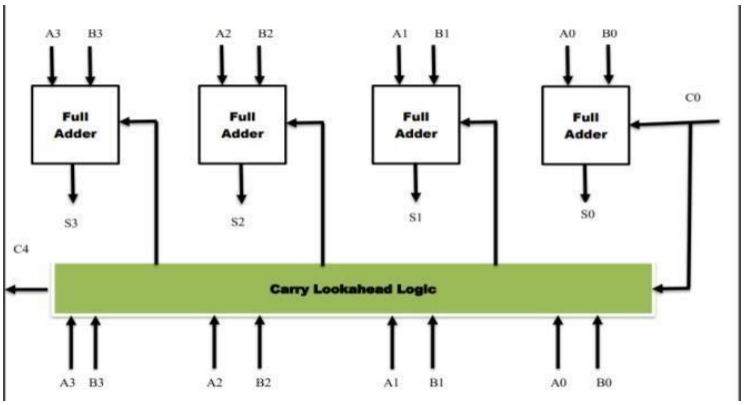

Fig1: 4-bit CLA block diagram

In Fig1 [1], C_0 input is given to both one-bit full adder and carry look ahead logic. As C_0 is applied to carry look ahead logic circuit the propagating carry inputs for other full adders is applied with reduced propagation delay. It will calculate other next stage carry inputs without waiting for previous stage output instead it will calculate as soon as C_0 is applied. This is one of the main advantages of Carry look ahead adder.

The output sum S_i, and carry C_i, can then be expressed as:

- $S_i = P_i \oplus C_i$ (a)
- $C_i+1 = G_i + (P_i * C_i)$ ---------- (b)

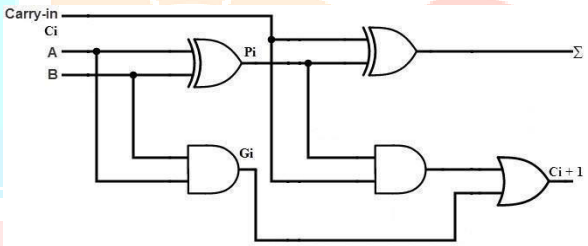

Fig2: Carry generate and propagate circuit using logic gates

The AND, OR and XOR gates needed to calculate the single-bit generate and propagate signals using two inputs, i.e., A_i and B_i. From Fig2 [5], the equation for Carry generate and propagate can be written as,

- $G_i = A_i B_i$ where G represents carry generator
- $P_i = A_i \oplus B_i$ where P represents carry propagator

Based on equation (b), the carries of the first four bit are as follows: $C_1 = C_0P_0 + G_0$ (1)

$C_2 = C_1P_1 + G_1$ ..... (2)

$C_3 = C_2P_2 + G_2$ ..... (3)

$C_4 = C_3P_3 + G_3$ ..... (4)

Substituting C_1, C_2, and C_3 in equation (1) to (4) the following equations are obtained: $C_1 = C_0P_0 + G_0$

$C_2 = C_0P_0P_1 + G_0P_1 + G_1$

$C_3 = C_0P_0P_1P_2 + G_0P_1P_2 + G_1P_2 + G_2$

$C_4 = C_0P_0P_1P_2P_3 + G_0P_1P_2P_3 + G_1P_2P_3 + G_2P_3 + G_3$

B. 32-bit Carry look ahead adder

Fig 3 [4] shows a 32-bit carry-lookahead adder composed of eight 4-bit blocks. Each single block represents a 4-bit CLA which computes the sum of 4-bit at faster rate and also calculates carry propagate and generate which passes to the next stage. The carry in is applied to the 4-bit CLA from logic circuit.

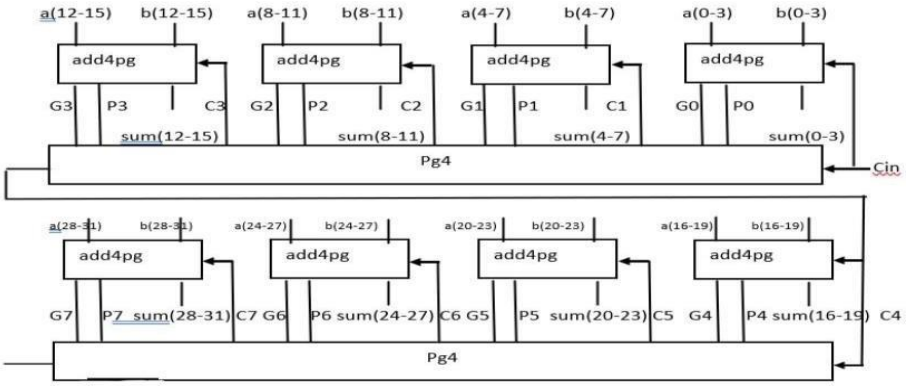

Fig3: 32-bit CLA block diagram

III. IMPLEMENTATION

A. Implementation of 4-bit carry-lookahead adder

In Electric binary, the design of a 4-bit Carry Look-Ahead adder has been designed as shown in Figure9. The proposed CLA technique computes carry-out terms using the carry propagate and generate. The suggested 4-bit CLA architecture's performance parameters were simulated and validated by using Electric VLSI design system. Simulations were run using Electric VLSI design system with a 45 nm technology and LT Spice software in order to accomplish this.

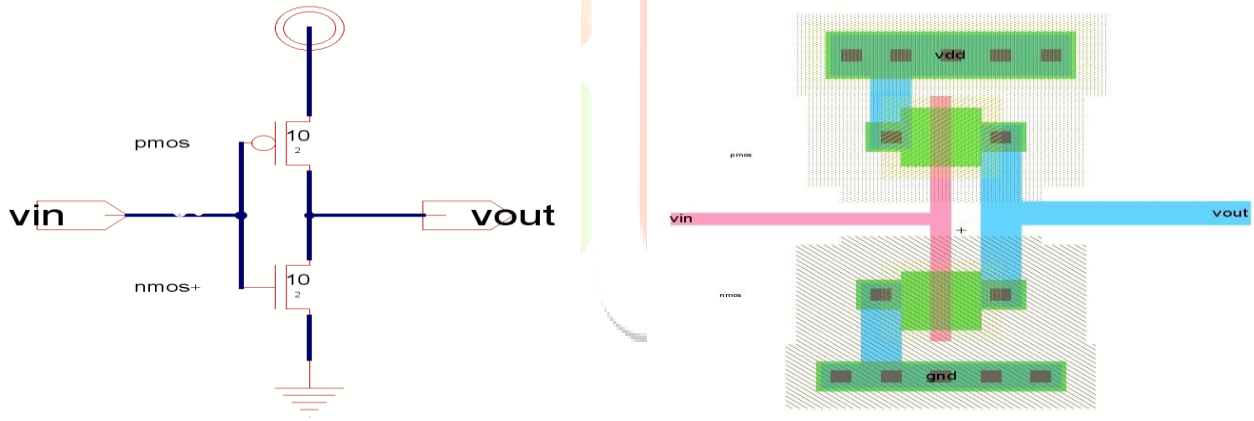

Fig4: Schematic and Layout of NOT gate

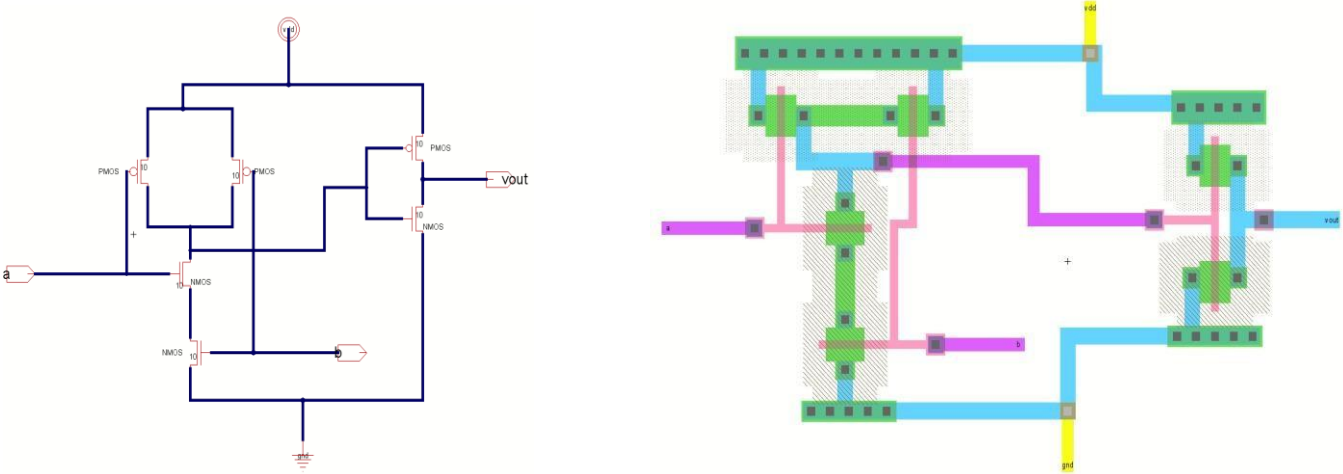

Fig5: Schematic and Layout of AND gate

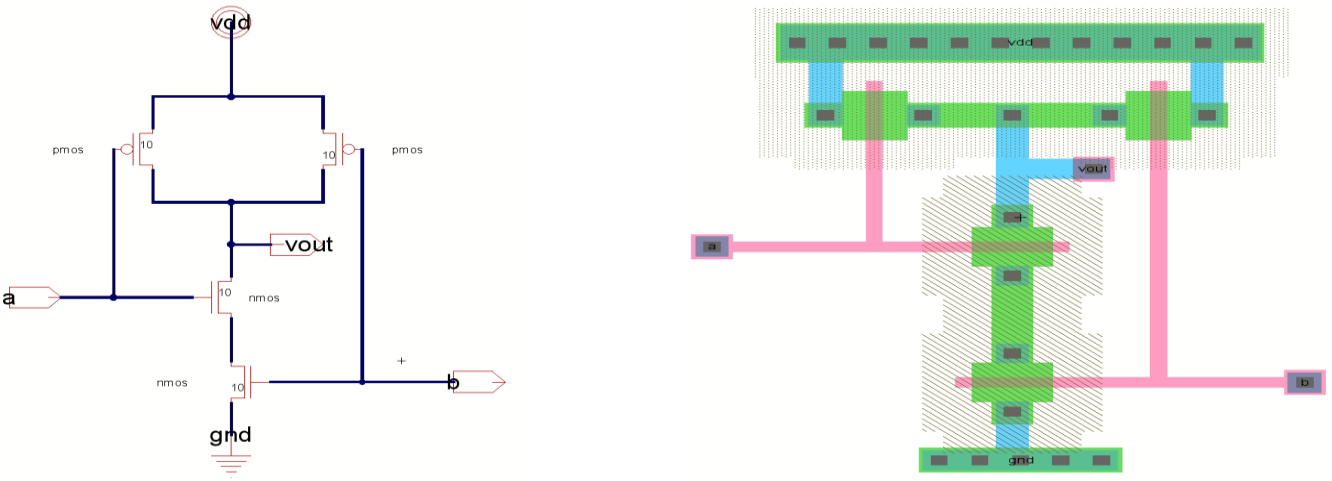

Fig6: Schematic and layout of NAND gate

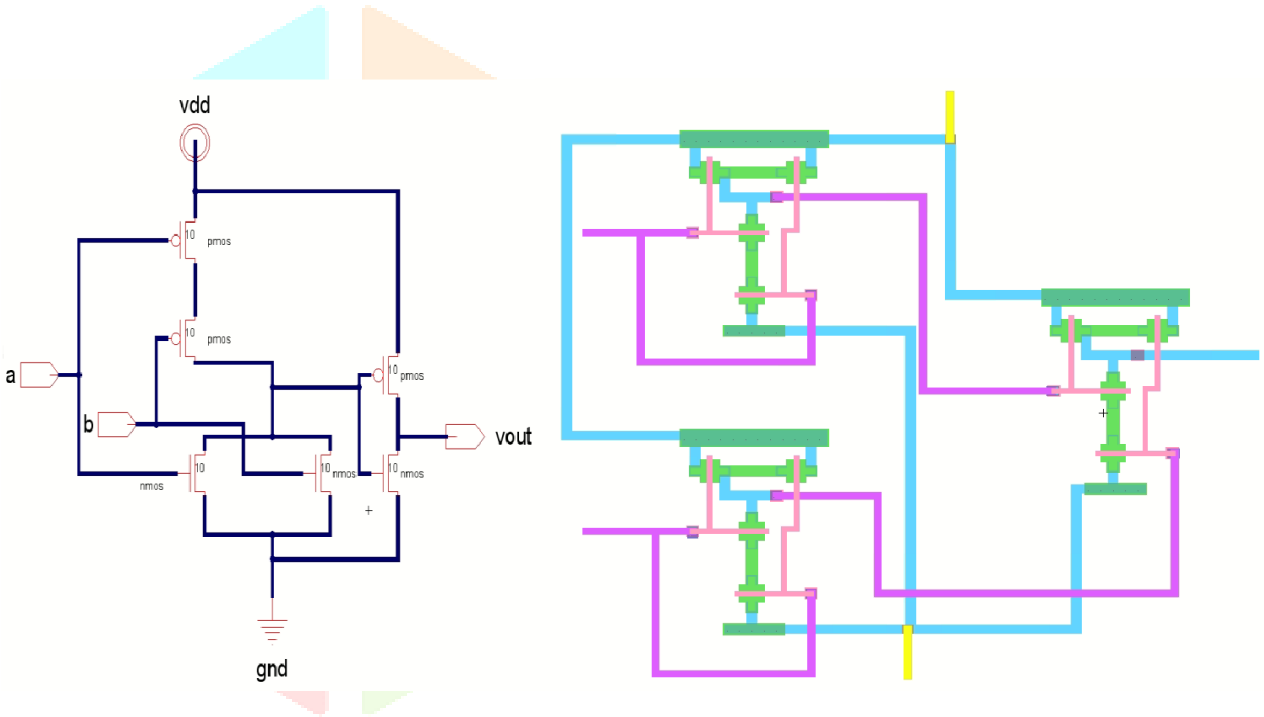

Fig7: Schematic and layout of OR gate

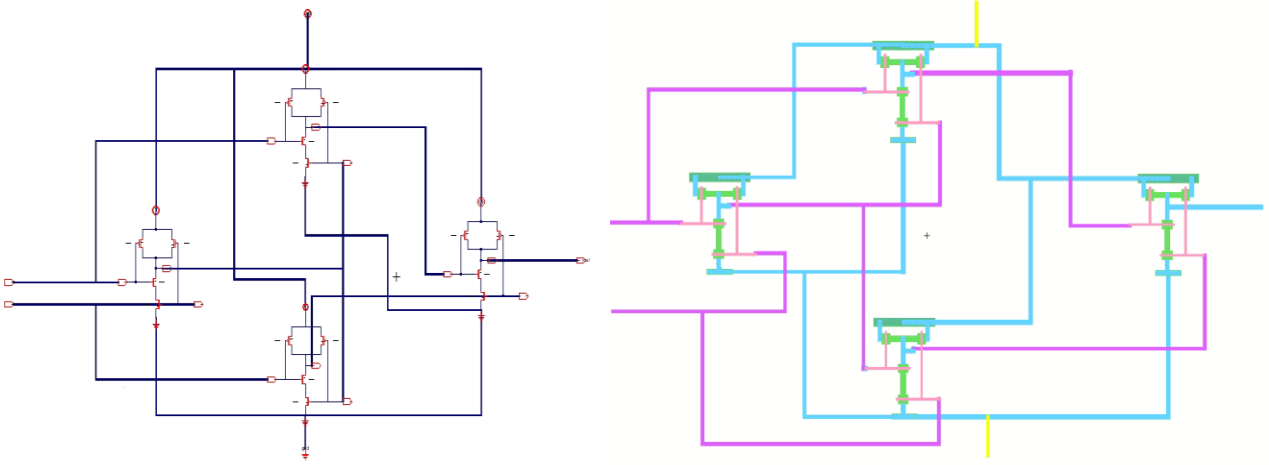

Fig8: Schematic and layout of XOR gate

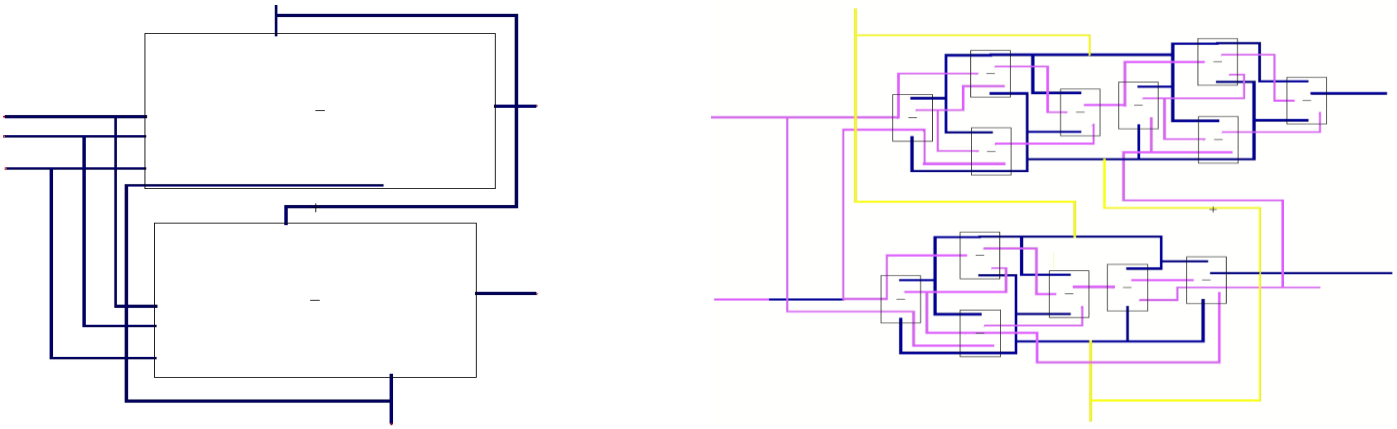

Fig9: Schematic and layout of 1-bit full adder

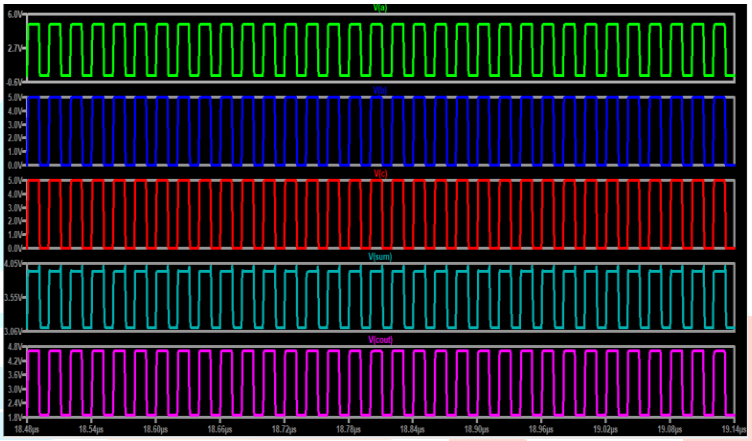

Fig10: Transient analysis of 1-bit full adder

The above schematic from Fig5 to Fig8 has been used to compute one-bit adder, generate and propagate circuit and logic circuit to produce carry out. Using all the schematics and layouts in Fig4, Fig5, Fig6, Fig7, Fig8 and Fig9 a 4-bit CLA schematic and layout is designed.

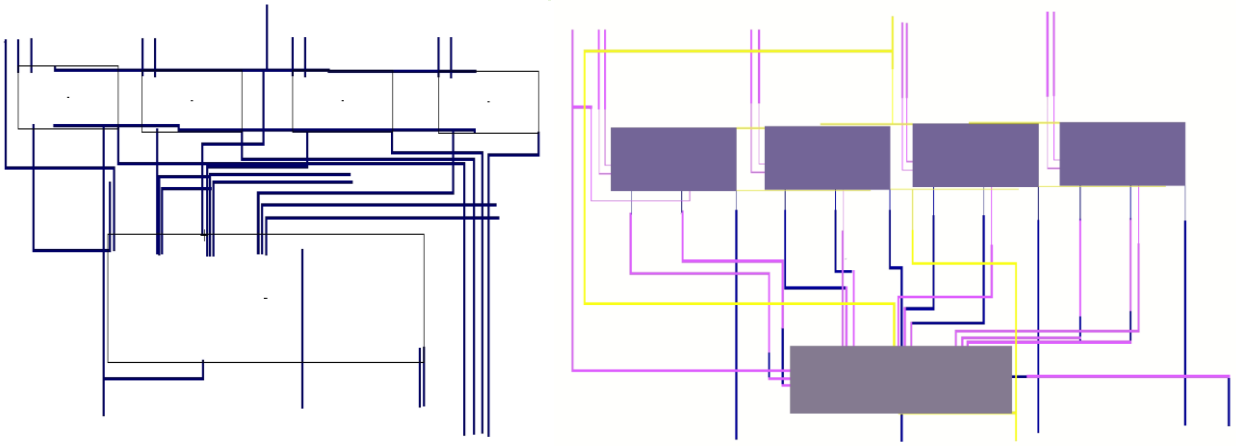

Fig11: Schematic and Layout of 4-bit CLA

The Figure12a and 12b shows the transient analysis of 4-bit Carry look ahead adder which is simulated in LT spice using Electric binary at 45nm technology.

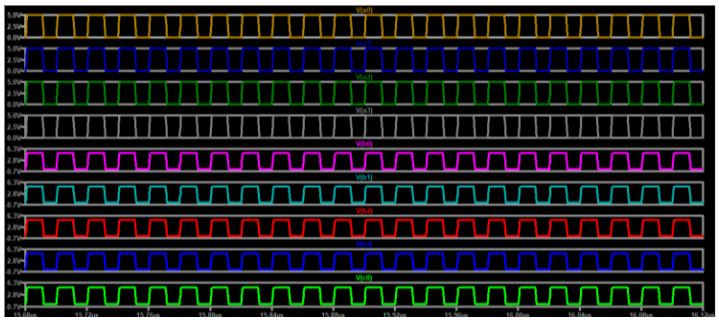

Fig12a: Inputs for 4-bit CLA

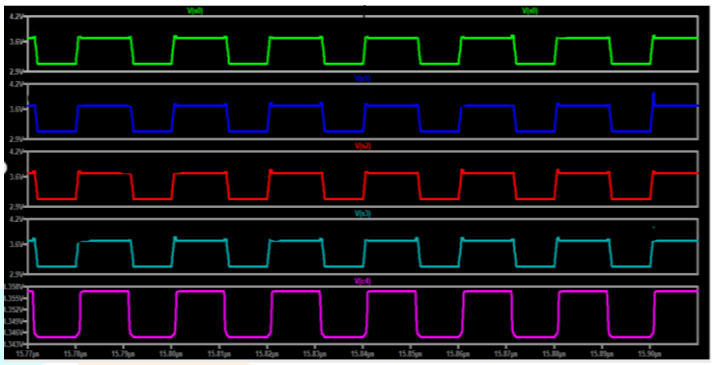

Fig12b: Output Transient Analysis of 4-bit CLA

B. Implementation of 32-bit CLA using Electric

In Electric VLSI Design System, the design of a 32-bit Carry Look-Ahead (CLA) has been designed using eight 4bitCLA along with Carry generation and propagation circuits. The below figure13 shows the schematic of 32-bit CLA.

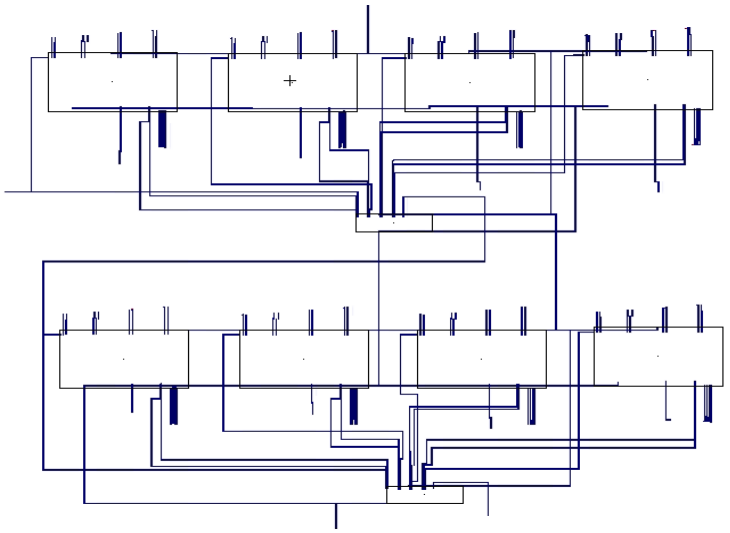

Fig13: Schematic of 32-bit CLA

The Figure14a and 14b represents the transient analysis of 32-bit Carry look ahead adder which is simulated in LTspice using Electric binary at 45nm technology.

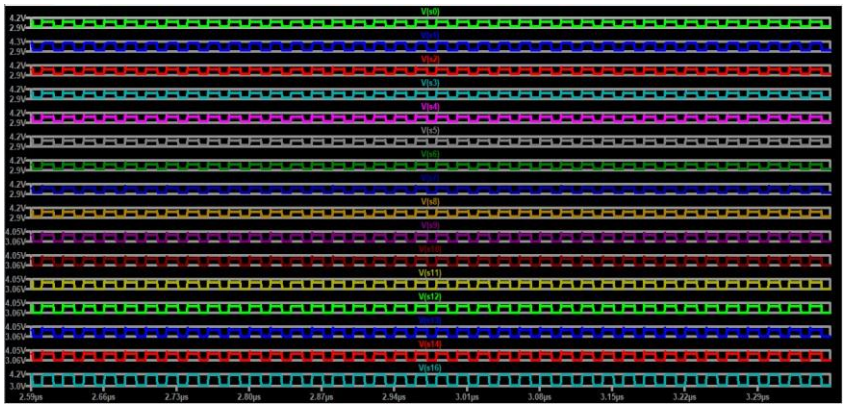

Fig14a: Output Transient Analysis of 4-bit CLA [s0 – s16]

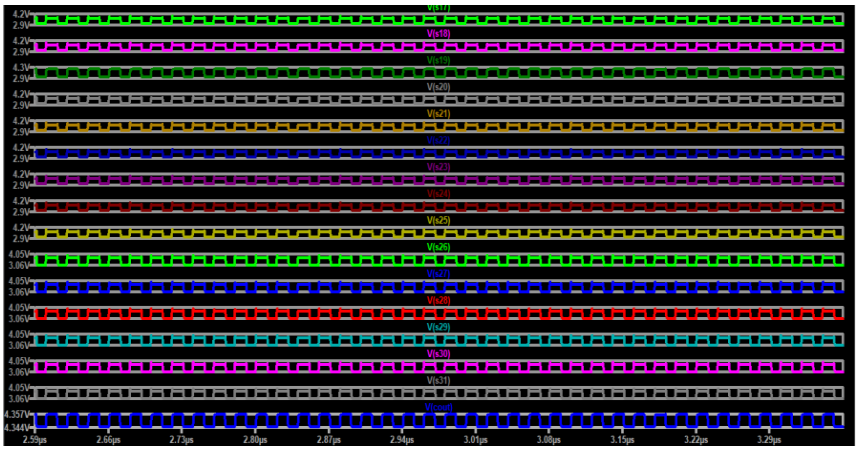

Fig14b: Output Transient Analysis of 4-bit CLA [s17- s32, cout]

IV. CONCLUSION

Carry look ahead adder employed the great importance to reducing carry propagation delay of the adder. Though compared with other different logic design approaches CLA logic calculates carry propagating to the next stage as soon as inputs are applied. The schematic of 4-Bit adder and 32-bit adder is implemented using Carry Look Ahead logic designed using electric binary 9.07 tool.

V. REFERENCES

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