Design and Analysis of Chip Based Demultiplexer Using VLSI Design System

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***Abstract*—This paper discusses the design of an Integrated Circuit (IC) based for a Demultiplexer. The based was designed by using an open source software namely Electric VLSI Design System as the Electronic Design Automation (EDA) tool. In order to produce the based, the basic knowledge of fabrication process and IC design rules are expounded. The complete based of the Demultiplexer was designed based on its schematic circuit, which consists of NOT gates, 2-input NAND gates, 3-input NAND gates, 4-input NAND gates, 2-input AND gates and 3-input AND gates. The based had undergone Design Rule Check (DRC) set by the Electric VLSI Design System to check for any design rule error. Both based and schematic circuit of the Demultiplexer were then simulated through Based versus Schematic (LVS) to ensure they were identical. LT spice is used as simulator to carry out the simulation work and verify the validity of the function. The simulation output indicated that results of the based and schematic circuit for Demultiplexer were essentially identical and matches the theoretical results.**

***Index Terms*—Demultiplexer, schematic circuit, IC based, electric VLSI Design System, NAND gates, AND gates and simulation output**

I. INTRODUCTION

Electronic devices have been widely used in many different fields and the size of these devices has been gradually reduced. An example of this is the mobile phone which is made smaller to enhance user's mobility and usage time. These are the contribution of integrated circuit (IC) technology. With this technology, the modern devices have been reduced to convenient sizes. Besides that, mass production of IC has lowered the cost of production and made most electronic devices affordable. Today, an IC is smaller than a coin and can hold millions of transistors. Hence, further research in the design of IC is important to enhance the production of a more efficient and viable IC.

The main objective of this paper is to design an IC layout of a 7-segments decoder by Electric VLSI Design System. It is a free open source EDA system that provides service in handling IC layout, schematic drawing, textual hardware description language, and other features [1]. By using this software, a micrometer sized IC can be easily designed due to the availability of various features that can be used to design and check the IC based. Moreover, Electric VLSI Design System also allows the schematic and based design to be done in a systematic and efficient manner, thus saving time and reducing the production cost of the IC chip.

There are different technologies to construct integrated circuits such as bipolar integrated technology, NMOS technology and CMOS technology. In this project, CMOS technology is used. The main reason in using CMOS technology is due to its scalable high noise immunity and low power consumption. Basically, CMOS technology uses both NMOS and PMOS, which means only either one of both types of transistors will be ON at a time during the operation. Thus, CMOS IC consumes less power as power is used only when the NMOS and PMOS transistors are switching between on and off states [2].

II. LITERATURE REVIEW

A. 7-Segments Demultiplexer

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The main objective of this paper is to design an IC based of a 7-segments Demultiplexer by Electric VLSI Design System. It is a free open source EDA system that provides service in handling IC based, schematic A 7-segments Demultiplexer is able to convert the logic states of inputs into seven bits of outputs and displays in 7-segments display. It is used widely in devices where its main function is to display numbers from a digital circuitry. Examples of these devices includes calculators, displays in elevator, digital timers, digital clocks and etc. There are many types of Demultiplexer such as 2-4 Demultiplexer, 3-8 Demultiplexer and 4-16 Demultiplexer. Since there are ten decimal numerals (0–9) to be displayed in the 7-segments display, a 4-16 Demultiplexer was used.

The structure of a 7-segments display is shown in Fig.

1. It is used to display decimal numerals in seven segments and each segment is represented by an alphabet '*a*' to '*g*'. By setting the required segments to be turned on, the desired decimal numeral can be displayed on the 7-segments display. The logic diagram of 7-segments Demultiplexer is shown in Fig. 1.

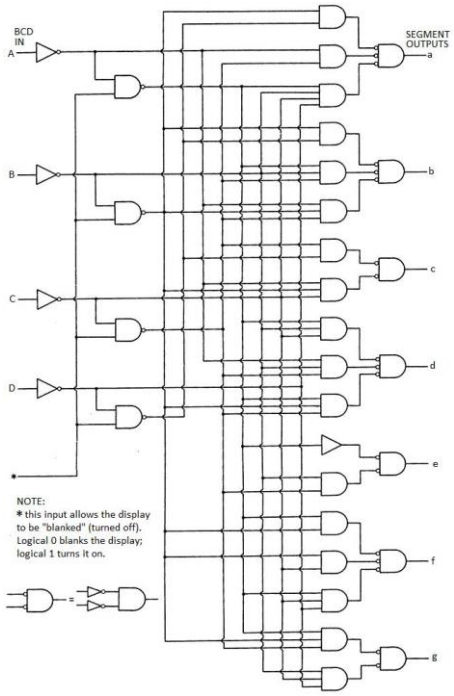

Figure 1. The logic diagram of a 7-segments Demultiplexer [3]

B. IC Design

IC based are built from three basic components which are the transistors, wires and vias. During the design of the based, the design rule has to be considered. Design rules govern the based of individual components and the interaction between those components. When designing an IC, designers tend to make the components as small as possible enabling implementation of as many functions as possible onto a single chip. However, since the transistors and wires are extremely small, errors may happen during the fabrication process. Hence, design rules are created and formulated to minimize problems during fabrication process and helps to increase the yield of correct chips to a suitable level. Therefore, it is important to adhere to the design rules during based design.

C. Physical Verification of Design [1], [4]

Physical verification is a process where an IC based design will be checked via EDA tools to ensure it meets design criteria and rules. The verification process used in this project involves DRC (Design Rule Check), LVS (Based Versus Schematic) and ERC (Electrical Rule Check). These are important procedures in IC based design and cannot be treated lightly.

i) Design Rule Check (DRC)

DRC is a verification process that determines whether the physical based of a chip design satisfies the Design Rules or not. It ensures that all the polygons and layers meet the manufacturing process rules that defines the limits of a manufacturing design such as the width and space rules. DRC is the first level of verification once the based is ready. In this verification stage, the connectivity and guidelines rules will be checked as well. DRC will not only check the designs that are created by the designers.

ii) Based Versus Schematic (LVS)

LVS is a process to check if a particular IC based corresponds to the original schematic circuit of the design. The schematic acts as the reference circuit and the based will be checked against it. In this process, the electrical connectivity of all signals, including the input, output and power signals to their corresponding devices are checked. Besides that, the sizes of the device will also be checked including the width and length of transistors, sizes of resistors and capacitors. The LVS will also identify the extra components and signals that have not been included in the schematic, for example, floating nodes.

iii) Electrical Rules Check (ERC)

ERC is usually used to check the errors in connectivity or device connection. It is an optional choice of checking and seldom used as an independent verification step. ERC is usually used to check for any unconnected, partly connected or redundant devices. Also, it

will check for any disabled transistors, floating nodes and short circuits. ERC is very useful in accelerating debugging problems such as short circuits as can speed up the design process.

III. METHODOLOGY

The schematic circuit of the 7-segments Demultiplexer was drawn and debugging process had been carried out to ensure the design is error free. In this project, the based of the 7-segments Demultiplexer was designed using Electric VLSI Design System to exploit its powerful editing tools.

Electric VLSI Design System is a high performance EDA tool that provides complete aids in designing the IC based. It integrates the schematic editor, circuit simulator, schematic driven based generator, based editor, based verification and parasitic extraction. Another advantage to Electric VLSI Design System is that it allows swapping between the designs data with other standard EDA tools in the industry. [1]

Besides that, LT spice IV simulation software was also used in this project. It is a high performance SPICE simulator that provides a schematic capture .

TABLE I. LIST OF FUNDAMENTAL RULE OF DESIGNING AN IC BASED [5]

Well	
Minimum well size	12λ
Between wells	6λ
Between N-well and P-well	0λ
Minimum well area	$144\lambda^2$
Polysilicon1	
Polysilicon1 width	2λ
Between polysilicon1s	3λ
Between polysilicon1 and metal	N/A
Minimum polysilicon1 area	$4\lambda^2$
Polysilicon2	
Polysilicon2 width	7λ
Between polysilicon2s	3λ
Between polysilicon2 and metal	N/A
Minimum polysilicon2 area	$49\lambda^2$
Metal1,2,3,4,5	
Metal width	3λ
Between metals	3λ
Between metal and other metal	N/A
Minimum metal area	$9\lambda^2$
Via1,2,3,4	
Via width	2λ
Minimum via area	$4\lambda^2$
Metal6	
Metal6 width	5λ
Between metal6s	5λ
Between metal6 and other metal	N/A
Minimum metal6 area	$25\lambda^2$
Via5	
Via5 width	3λ
Minimum via5 area	$9\lambda^2$

Table I shows the basic design rule in a list. As shown in Fig. 2, the minimum distance between two same metals or poly silicon's must be at least 3λ. Besides, the width of metal from 1 to 5 must be at least 3λ wide. Notice that in Table I, some parameter's rule are labeled as 'N/A'. This is because there are not such spacing rules. In other words, the respective components can be placed overlapping each other. Also, there are rules where the parameter is 0λ. This indicates that the respective components can be placed side by side without any space in between. There is also no minimum distance between vias or with other components listed in the table. This is because the vias available in Electric VLSI Design System are combined with 2 metals, covering every side of the vias. Therefore, before the vias can be placed nearer to each other, the metal surrounding it will connect each other first. The distance between the metal of vias has to obey the rules before the vias have the chance of contact. In other words, it also indicates that the minimum distance between vias or with other components can be determined through the metal's rule.

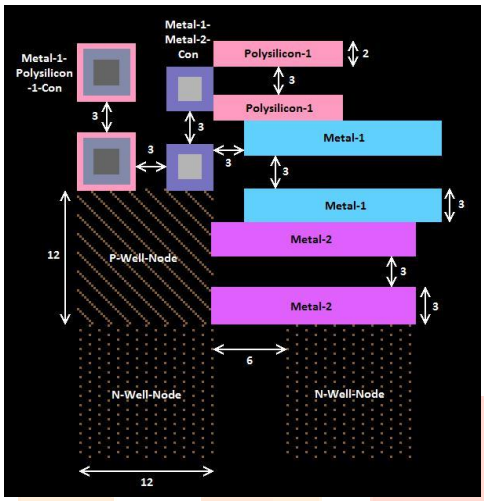

Figure 2. Fundamental rule of designing an IC based (All values are in lambda) [5]

IV. FINDINGS

In this project, an IC based of a Demultiplexer that displays the decimal numeral in 7-segments display was designed. It consists of NOT gates, 2-input NAND gates, 3-input NAND gates, 4-input NAND gates, 2-input AND gates and 3-input AND gates. The schematic circuits and based of all these gates were drawn and simulated using Electric VLSI Design System. Also, LT Spice was used as external simulator to generate the simulation waveforms.

A. 2-Input NAND Gates

Fig. 2 and Fig. 3 shows the schematic diagram and based design of a 2-input NAND gate using Electric VLSI Design System.

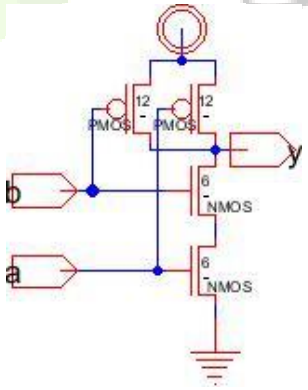

Figure 3. Schematic diagram of a 2-input NAND

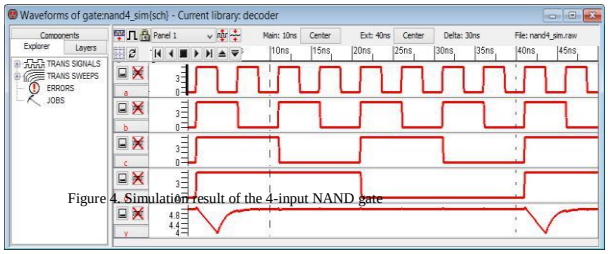

Figure 4. Simulation result of the 4-input NAND gate

D. 7-Segment Demultiplexer

All the schematic diagrams and baseds of the basic gates drawn have to go through the physical verification process before simulation. These are the essential procedures to ensure the validity outputs results of the system.

Based on the logic diagram of 7-segment Demultiplexer, the schematic circuit and its IC based was designed using Electric VLSI Design System tool, as shown in Fig. 4

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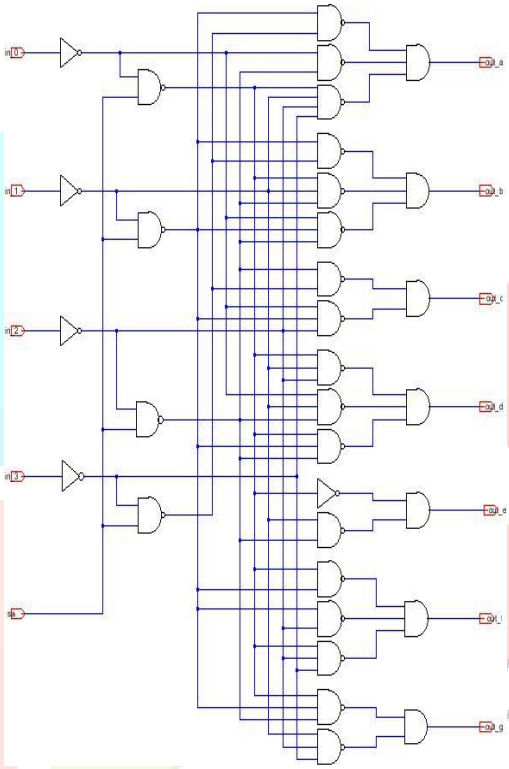

Figure 5. Schematic diagram of a 7-segments Demultiplexer

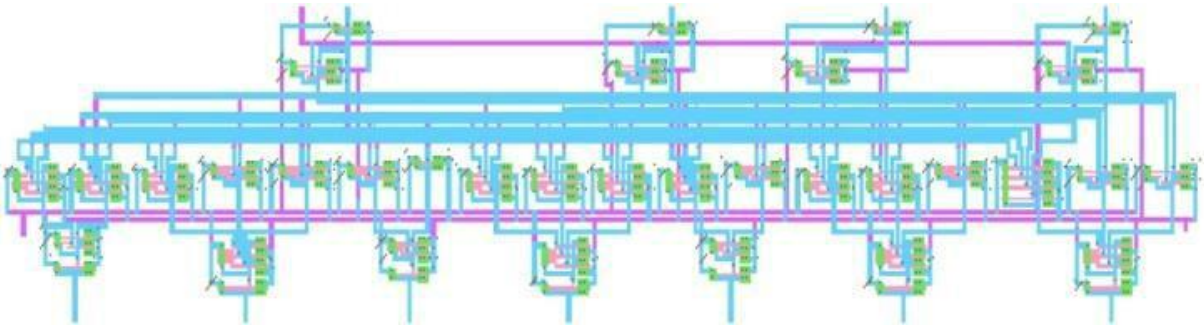

Figure 6. IC based design of Demultiplexer

However, Fig. 5 shows the icon view of the Demultiplexer with spice code, which is ready for simulation. It shows the inputs and outputs port and also the spice code that specifies the input pulses of the Demultiplexer for simulation. There are five inputs: ‘in_0’, ‘in_1’, ‘in_2’, ‘in_3’ and ‘sw’, where ‘in_0’ is the least significant bit and ‘in_3’ is the most significant bit. Since it is a 7-segment Demultiplexer, seven outputs will be needed. These outputs are labelled as ‘out_a’, ‘out_b’, ‘out_c’, ‘out_d’, ‘out_e’, ‘out_f’ and

'out_g'. Notice that there is a 'sw' input which represents the switch. When the switch is to '0', no matter what other inputs are, the outputs will always be '0'. When the switch is to '1', the outputs will be varied according to the binary combination of the inputs.

Fig. 6 is the simulation waveform generated with different inputs. It is known that as long as the 'sw' is off, the outputs will be '0'. This figure shows simulation waveform for when the 'sw' is off. In reference to the truth table of the binary-convert-decimal, the designed Demultiplexer is match with the theoretical work and said to function as expected

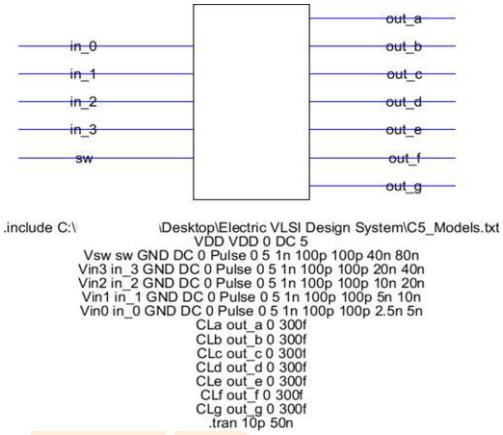

Figure 7. Icon of Demultiplexer and spice code

A. *Verification Process*

As mentioned earlier, physical verification process is an essential procedure. The schematic diagram and based design can be checked through DRC. It is recommended that the schematic diagram is free of warning and error before designing its based.

LVS is used to ensure that the schematic diagram and its based are identical. This process will check the number of exports, ports, transistor size between schematic and the based. Error may occur if they are not consistent.

While running the LVS, the library names for both schematic and based have to be same and place under the same group. This is to ensure that the software compares the correct library.

B. *Spice Code*

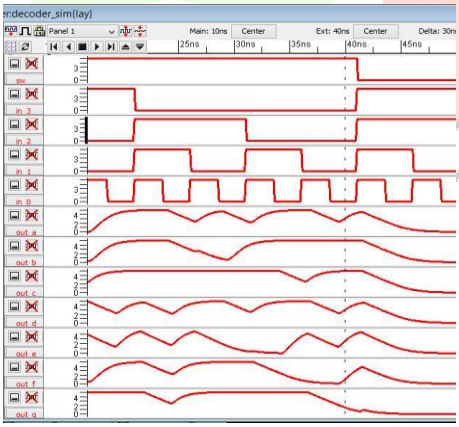

Figure 8. Simulation result of the 7-segments Demultiplexer

TABLE II. TRUTH TABLE OF BINARY-CONVERT-DECIMAL (BCD)

	INPUT				OUTPUT						
No	in_3	in_2	in_1	in_0	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1

5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

IV. TROUBLESHOOTING

In order to avoid inability to run the simulation, the following steps have to be taken:

A. Setting and Installation

Before start drawing the schematic circuit, all the setting of the Electric VLSI Design System must be done properly. These include the installation of external In Electric VLSI Design System, spice code is used as function to be read by LTspice in order to simulate the waveform. A proper and correct spice code will generate correct waveform through this simulator. Spice code is written and inserted in the icon view of the Demultiplexer before running simulation. It specifies the input pulses and all the ports of Demultiplexer. The code written must be consistent with the icon drawn.

V. CONCLUSION

In conclusion, 7-segments Demultiplexer IC is to display the numbers in 7 segments. It converts the binary input to 7 bits according to the input. The IC based of the Demultiplexer is designed and successfully proves that the output waveforms generated matches the theoretical Demultiplexer.

In addition, the open source Electric VLSI Design System is a user friendly software to be used in designing a based of 7-segments Demultiplexer. It is expected that the software is able to cope with more complex digital IC design with its suite of verification and design tools.

VI. REFERENCES

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