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Ternary Logic Applications in Basic Combinational Circuits

Abhiman Kumar [1(a)], Anurag Sah[1(b)], Dhanesh Prakash Gupta[1(C)], Dr. Asima Adak[2], Dr. Sriparna Bhattacharya (Mitra)[3], Dr. Anindya Sen[4]

[1(a),(b) & (c)] Students,[2]Assistant Professor,[3]Assistant Professor,[4] Professor

[1(a), (b) & (c)] Department of Electronics and Communication Engineering

[1]Heritage Institute of Technology, Kolkata-700107, India

Abstract: The algorithm for the function minimization of a multivalued, or radix >2, digital system is presented in this study. The suggested algorithm is illustrated here using a ternary digital system with radix=3, and a computer programme based on the algorithm is created in the form of a ternary map. The difficulty of minimising or reduction of the logic function grows as the system radix does. Higher radix make it harder to minimise the function design equation. The suggested programme was created to minimise the functions of ternary systems. The result is presented as Sum-of-Product (SOP) terms and includes all designed rules for ternary logic system architecture.. In contrast to the traditional binary digital system, ternary logic-based systems have alternative principles for minimization. The ternary digital system's output equation takes the form F = F2 + 1. Where F1 = 1's minterms and F2 = 2's minterms, respectively. The findings are evaluated on a programme and compared with a truth table for ternary half adders and full adders, and it is determined that the results are accurate.

Index Terms **– Logic Gates, Ternary Logic, Ternary K-MAP , Reduced gate .**

I. INTRODUCTION

The major goal of this study is to introduce ternary logic as a simpler and more energy-efficient alternative to binary logic because fewer gates are needed with ternary logic[1]. ALEXANDER provided a fantastic justification for the use of any switching circuits, pointing out that their natural base, e = 2.71828, is a very effective radix [2]. Thus, it can be observed that radix 3 is a more effective method than radix 2 for implementing digital systems. Three different values have been switched in ternary logic. By adopting a ternary logic architecture, sequential as well as combinational circuit implementation is both feasible and realised [3, 4]. When compared to binary logic digital systems, ternary logic digital systems can offer some significant advantages. These benefits include decreased interconnection requirements, which indirectly reduces chip space. Additionally, by adopting ternary logic systems, the number of functions is increased [5]. Many-valued logic is a propositional calculus in the Multi-valued logic where there are more than two truth values. "True" and "false" were the only two allowed values in the past.An n-valued logic for n more than 2 is an easy extension to conventional two values logic. The three valued logic, the finite value with more than three values, and the infinite (for example, fuzzy logic) logic are the most common in the literature[6-7]. Compared to standard binary logic design, the goal of ternary logic design is to enable more complex and efficient information processing. Ternary logic design does this by adding a third possible state to the binary logic's two (0 and 1) possible states. In ternary logic, the third state is often denoted by the number "2". Designing ternary digital circuits, which used three-state logic gates to represent three distinct states: high, low, and open, was one of the first uses of ternary logic. Ternary logic was thought to be a means to make digital circuits more efficient by enabling more complicated operations to be carried out with fewer components[8].. Ternary logic, which employs three values—typically denoted as 0, 1, and "unknown" or "indeterminate"—can be advantageous in some circumstances when binary logic, which employs only two values—typically denoted as 0 and 1—might not be sufficient. Ternary logic has the advantage of being able to express more states than binary logic, which is sometimes advantageous. For instance, ternary logic can be used in some computing systems to represent "uncertain" or "unknown" results that may result from defective sensors or other unforeseen events. Ternary logic can occasionally make circuits simpler and require fewer logic gates to perform particular purposes. This is especially helpful when designing hardware because fewer components mean lower costs and better performance. Ternary logic frequently handles circumstances where some input values are absent or unclear, making it more fault-tolerant than binary logic. This can be helpful for safety-critical systems, where it's crucial to make sure the system can keep running even when there are defects or faults[9–10].

2. EXPERIMENTAL DETAILS

The main qualities that are utilised to define and assess ternary logic circuits like the AND, OR, and NOT operations are known as the parameters of ternary logic design. the fundamental components of ternary logic circuits, which carry out particular logical operations on a single or a number of inputs. Ternary inverters, ternary AND gates, and ternary OR gates are examples of common ternary logic gates. the particular logical operations, including addition, subtraction, and comparison, that can be carried out utilising ternary logic. Combinations of ternary logic gates and other parts can be used to implement these functions. selecting the proper gates, functions, and levels in order to construct ternary logic circuits that have the functionality required. Generally speaking, ternary logic design parameters are used to characterise, assess, and direct the design process of ternary logic circuits. Designers can produce ternary logic circuits that precisely match the needs of particular applications by carefully choosing and optimising these characteristics.[11].

2.1 Ternary Algebra

Z = 0 and 1 represent the logic level in a binary logic system, where 1 denotes truth and 0 denotes falsity. Z = 0 and 1 denote the values in a ternary logic system. The three voltage levels in ternary voltage switching circuits are represented by 0, 1, and 2. Here, 0 denotes a low potential, 1 an intermediate potential, and 2 a great potential. Let's take a look at a system Z whose constituents, referred to as propositions or assertions, are valued in the range of 0, 1, and 2. The definitions of the addition (+) and multiplication (.) operations in Z are given in [12].

- $x+y=\max(x,y)$
- $x\cdot y=\min(x,y)$
- **Commutative:**
  - $x+y=y+x$
  - $x\cdot y=y\cdot x$
- **Associative:**
  - (x+y)+z=x+(y+z)
  - x.(y.z)=(x.y).z
- **Distributive:**
  - x+yz=(x+y)(x+z)
  - x(y+z)=x.y+x.z
- **Absorption:**
  - x+x.y=x;
  - x.x=x;
- **Idempotent:**
  - x+x=x;
  - x.x=x;
- There are some law which are used to minimize the ternary logic system [13] this are
  - x•0=0
  - x•2= x
  - x+0= x
  - x+2= 2

There exist $3^3= 27$ different unary functions on Z to Z.We single out them and denote [14] as shown in Table I.

TABLE I

x	$x0$	$x1$	$x2$	$x01$	$x12$	xx	$x\Delta$
012	200	020	002	220	022	012	222

Table I of unary function shows that

- $x^0 + x^1 + x^2 = x^\Delta$
- $x^{01}=x^0 + x^1$
- $x^{02}=x^0 + x^2$
- $x^1=x^{01} .x^{12}$

2.2 Function Mininization

According to the priority cost metrics, an output functional set has been pared down to its most basic form. Based on how closely the remaining reduced functional sets resemble the minimal functional set, they are rated. According to the absolute functional set, the degrees show the number and order of metric matches for each function. Higher degree-related duties must have satisfied any lower degree-related criteria. Product term equivalence has the coarse or lowest degree, followed by MIN-literal matching, and equivalent fundamental gate quantity has the highest degree.. Expressions that have been shrunk to their very tiniest form are said to as being in the greatest or finest degree. However, for a thorough evaluation of the algorithms and methods, general observations are as helpful with such information. Expressions with an equivalent number of product terms are further separated by the total number of product words in the expression. In such cases, the lowest value expressions result in the best reductions. A product term's fan-in requirements make up its size, which is determined by adding the MIN-literal for each vertex and one for the term's constant coefficient. The product term is said to be independentof the related vertex and its MIN-literal is subtracted from the product term when a MIN-literal spans all p logical values. Mining the constant coefficient and the MIN-literals is not necessary for product terms with constant coefficients equal to the greatest logical value p-1 [15]. The Quine-McCluskey approach, the Scheinman's Binary method, the Map reduction technique, and other methods have all been suggested for reducing ternary equations. The use of the MAP method to simplify or reduce ternary equations is the only application covered in this work. For the purpose of minimising the ternary function, there is a set of guidelines or a methodology for linking neighbouring cells. :-

1) The group of arrays of 3 × 1, 3 × 2, 3 × 3 cells can be formed to provide the output values coincide with the values of one of the inputs.

2) It is permitted to join (properly) adjacent cells with equal output values

3)Multiple uses of cells for different arrays are permitted.

4) Cells with the output value 2 can be considered as "don't care" for the formation of arrays with the output value 1. Output equation of ternary digital system is in the form of F1 and F_2 terms i.e.

$$F = F_2 + 1\bullet (F_1)$$

Where, F_2 = 2's minterms

F_1= minterms

- Two variable map can be represent as shown below in fig.1 where fif.2 represents the corresponding output values for its related input.

2.3 TERNARY TWO VARIABLES MAPS REPRESENTATION

TABLE II

	0	1	2
0	x_1	x_2	$x3$
1	x_4	x_5	x_6
2	x_7	x_8	x_9

Values x_1, x_2.... x_9 in Fig. 1 represents theoutput of the digital system. These values may be 0, 1and 2. It may be possible that it is don't care as well, here don't care is represented by "×". All the rules of map reduction can be applicable for two variable reduction techniques. Following are some example for two variable map reductions

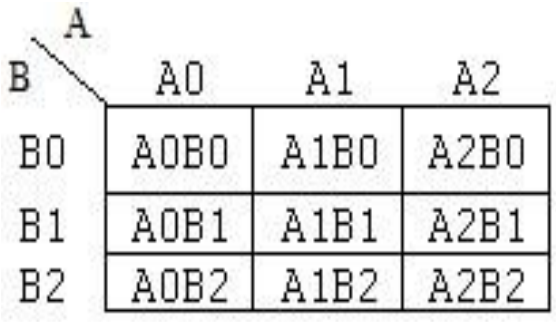

Fig. 1 Ternary Two Variable Maps

Example 1:- Let's take half adder, which have the input to be "A", "B" and output SUM is "Z" and CARRY is "C". The Truth table for half adder is shown in table III.

3. RESULTS AND DISCUSSIONS

Ternary Logic has been used to construct combinational circuits like the Half-Dder and Full Adder. Even yet, while building ternary logic circuits, design constraints are restrictions or demands that must be taken into account. These limitations may affect the final design's cost, performance, and dependability. However, using ternary logic, it may be possible to create both half adders and full adders.

3.1 Half Adder implementation using ternary logic

TABLE III

TRUTH TABLE FOR HALF ADDER

INPUT		OUTPUT	
A	B	SUM	CARRY
		Z	C
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

The map for the table III is given in figure 2

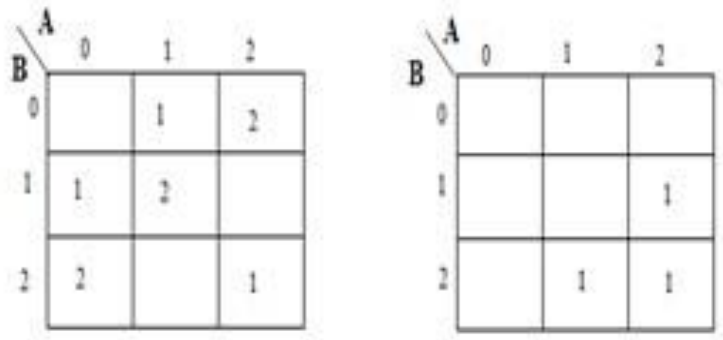

Fig. 2 Map for SUM And Map For CARRY

In fig. 2 There is not any group can form. So directly we can write equation for SUM and CARRY as

$$SUM = A^2B^0 + A^1B^1 + A^0B^2 + 1 \bullet (A^1B^0 + A^0B^1 + A^2B^2) \quad (26)$$

$$CARRY = 0 + 1 \bullet (A^2B^1 + A^1B^2 + A^2B^2)$$

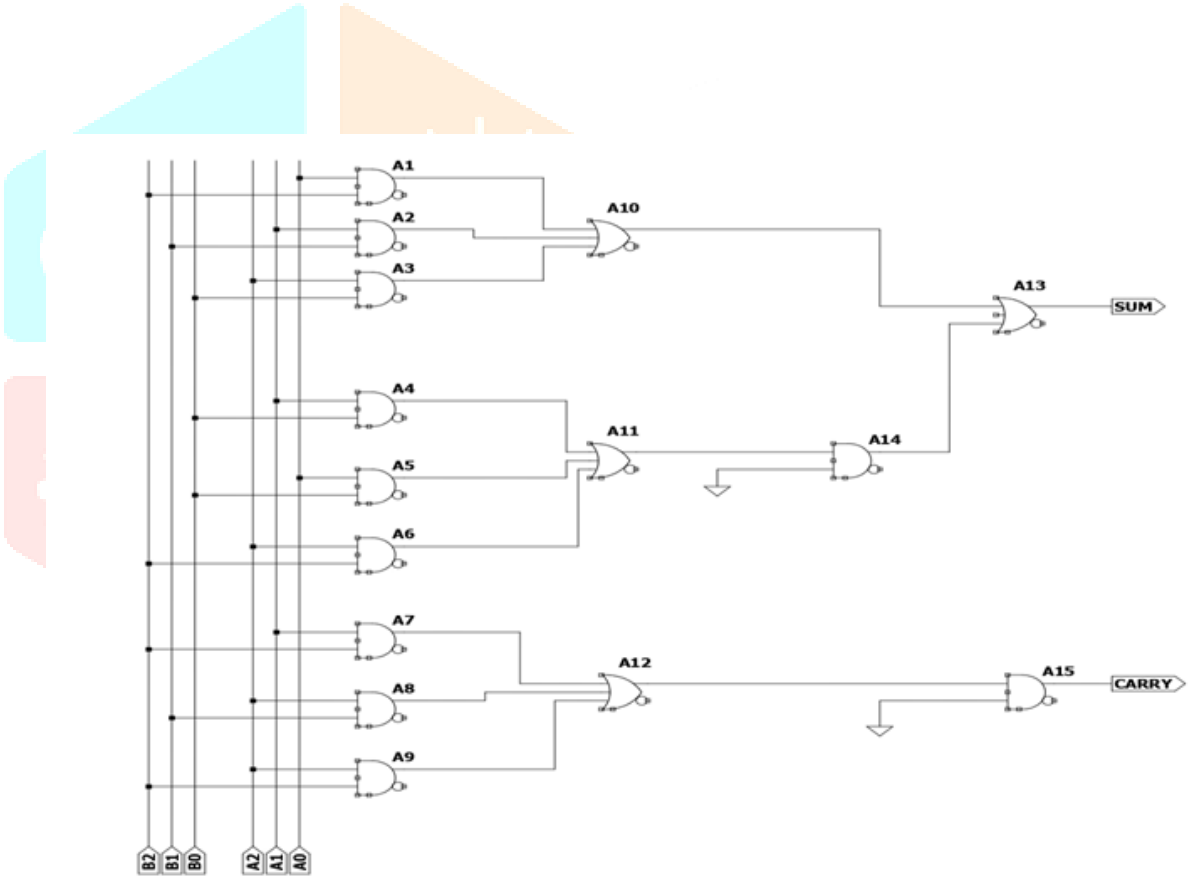

Fig 3: Half Adder Circuits using Ternary logic

3.2. Full Adder implementation using ternary logic

For three-variable functions can be draw as three- dimensional map as shown in Fig. 9. But it is very difficult to use this map for the performing operations so it is more convenient to use the two-dimensional map shown in Fig. 10. In this method of using two-dimensional map is similar to the two variables. Fig.4. shows grouping of consequent six 2's and three 1's combination for three variable map.

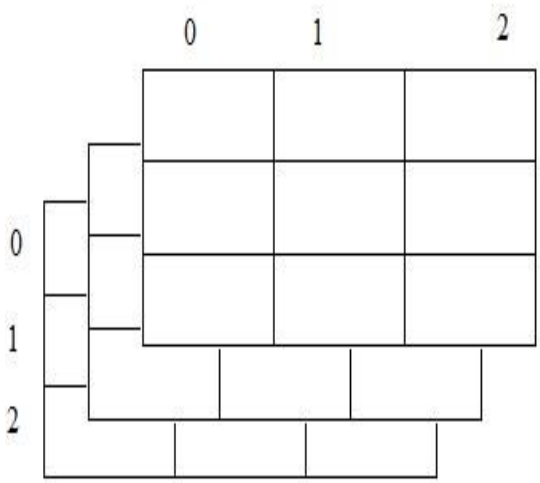

Fig. 4 Map Three Dimensional Three Variable Maps [13]

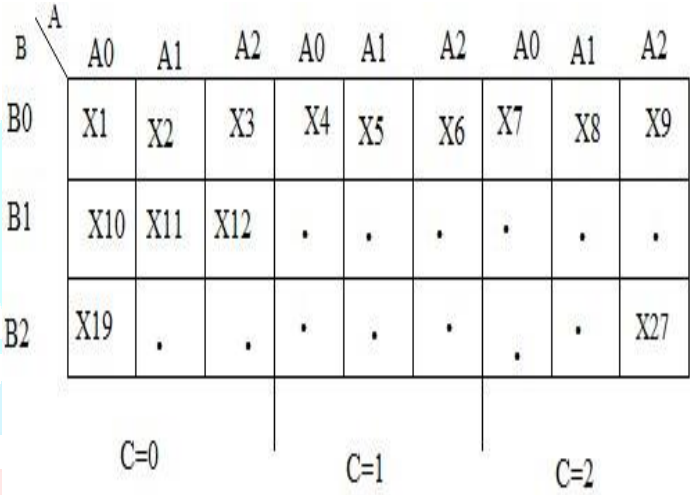

Fig.5 Two Dimensional Three Variable Map [13].

In fig.5 values x_1, x_2.... x_9 represents theoutput of the digital system. These values may be 0, 1and 2. It may be possible that it is don't care as well.

Example 1:- Let's take full adder, which have the input to be "A", "B" and output SUM is "Z" and CARRY is "C". The Truth table for full adder is given in table IV. The map for sum is representing as shown in fig. 6.

TABLE IV

TRUTHTABLEFORFULLADDER

INPUT			OUTPUT	
A	B	C	SUM	CARRY
			Z	C
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	1	0	1	0
0	1	1	2	0
0	1	2	0	1
0	2	0	2	0
0	2	1	0	1
0	2	2	1	1
1	0	0	1	0

1	0	1	2	0
1	0	2	0	1
1	1	0	2	0
1	1	1	0	1
1	1	2	1	1
1	2	0	0	1
1	2	1	1	1
1	2	2	2	1
2	0	0	2	0
2	0	1	0	1
2	0	2	1	1
2	1	0	0	1
2	1	1	1	1
2	1	2	2	1
2	2	0	1	1
2	2	1	2	1
2	2	2	2	2

From fig.6 we see that there is not any possibility for grouping the element so directly we can write the equation for sum.

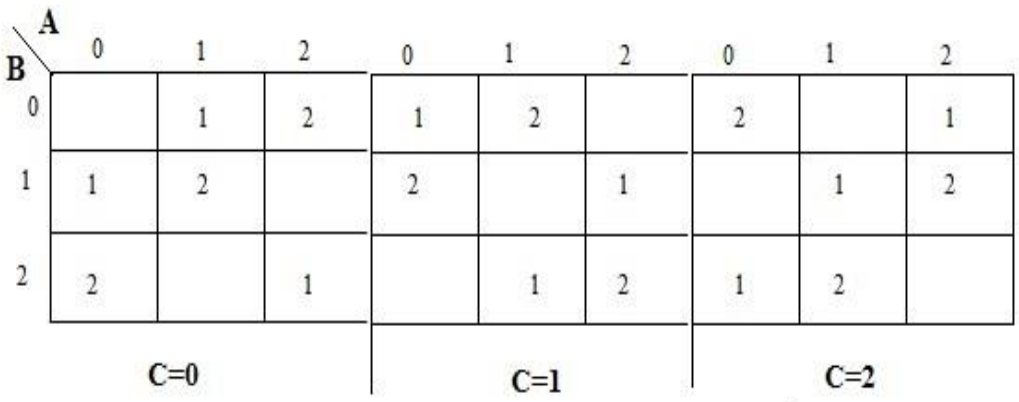

Fig. 6 Map for Full Adder SUM

SUM = “A2B0C0 +A1B0C 1+A0B0C2+ A1B1C0+
A0B1C1+A2B1C2 +A0B2C0 +A2B2C1+ A1B2C2 +1• (A1B0C0+A0B0C1+A20B0C2 +
A0B1C0 +A2B1C1 + A1BC2+A2B2C0
A1B2C1+0B2C2)”

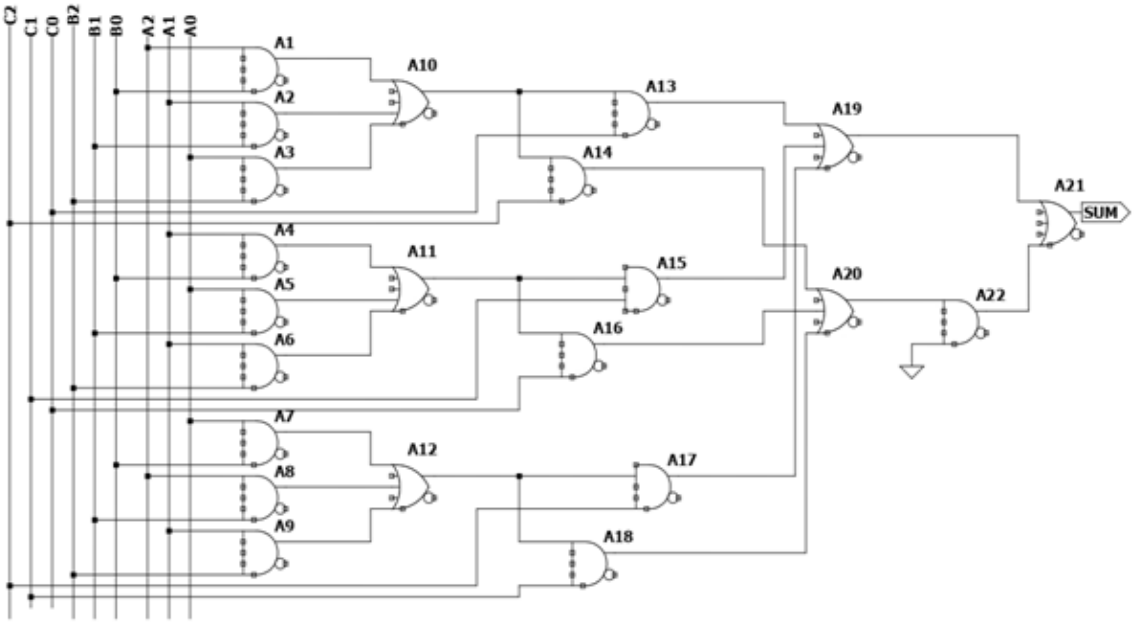

Fig 7: Full adder (sum) using ternary logic

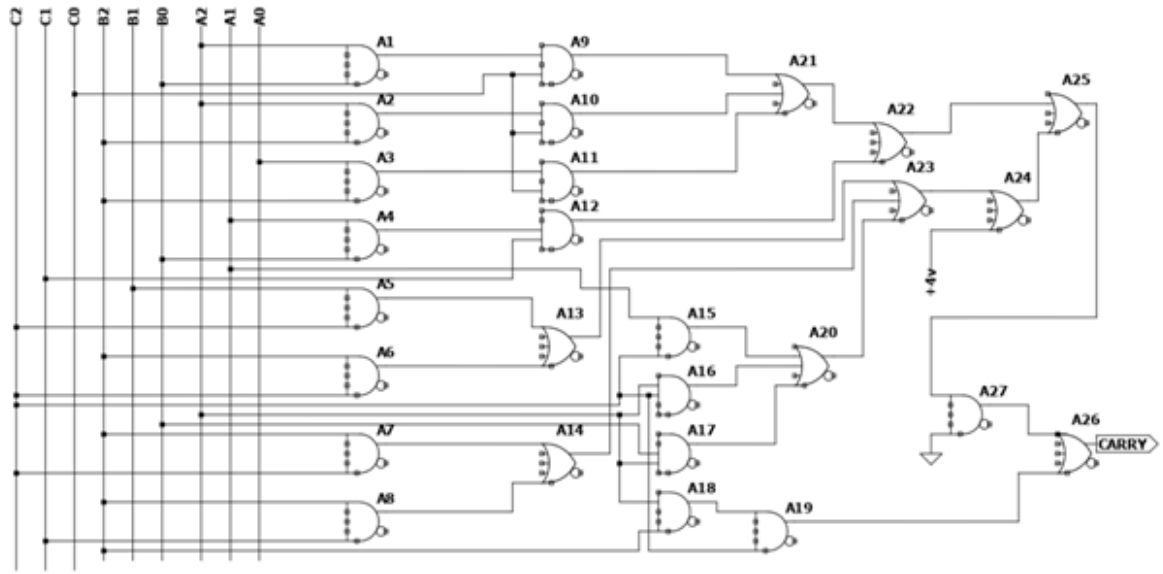

Fig 8: Full adder (carry) using ternary logic

In summary, while ternary logic can have certain advantages over binary logic, implementing it in a machine can pose several complications, such as lack of standardization, increased complexity, limited availability of components, compatibility issues, and difficulties in design and testing.

4 CONCLUSION

A viable replacement for the traditional binary logic design method is ternary logic. Utilising the advantages of ternary and binary logic gates, one can increase performance in terms of calculation speed and power consumption. Higher processing rates could be attained by raising the present logic levels. We have used a method to lower the gate count in this research. The key benefits of theternarylogic are that it uses 50% less power than theternarylogic while simultaneously requiring fewer computing steps, smaller chips, and faster chips. As a result, entire adder and multiplier circuits in data paths can benefit from good speed and power consumption characteristics when ternary logic gate design technique is integrated with the traditional binary logic gate design technique. MVL systems have been simulated using the VHDL simulator, which provides sufficient details to validate functionality and time requirements. A streamlined solution is produced via ternary function minimization using the map approach. This paper explains how to write the ternary k-MAP equation. The equation can be mapped using the computer-based programming software tool. The computer-based programming tool can accommodate up to 'N' variables. Future research in the design of combinational circuits employing ternary logic will focus on a number of different topics. One area is the creation of new methods and algorithms for constructing circuits with greater complexity and performance. The investigation of ternary logic's application in different digital circuit types, such as sequential and memory circuits, is another topic.

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