LOW POWER-AREA DESIGN OF FOUR BIT ARITHMETIC AND LOGICAL UNIT (ALU) IN CADENCE VIRTUOSO PLATFORM

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***Abstract*—** In order to endeavor in VLSI Technology, we have to keep in mind about Moore's law which states that in every 18-month number of transistors gets doubled on a chip. The purpose of this paper is to design Arithmetic and Logical unit (ALU) which have better performance in terms of power and area. ALU is the backbone of any processor, we have performed the Arithmetic operation like an adder, subtractor, multiplexer etc. & logical operations like AND, OR, XOR, Inverter, Binary to Gray, 1's complement of the number etc. The entire simulations have been done on 180 nm single n-well CMOS bulk technology, in the virtuoso platform of cadence tool with the supply voltage 1.8V and frequency of 4.07MHz.

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Index Terms*— *Adder, ALU, VLSI, CMOS, Low power, one's complement, multiplexer

I. INTRODUCTION

The ALU is a fundamental building block (core component) of the central processing unit (CPU) and is a critical component for microprocessors. It is an extremely versatile and useful device since it performs arithmetic and logical operation and comes in a single package. Nowadays ALU is getting petite and more convoluted to make an all-powerful but smaller computer but there are some parameters like IC fabrication technology, designer productivity, and design cost, slow down the development of petite and more convoluted IC chip. VLSI designs can be marked at different design levels, being the architectural, circuit, layout, and the process technology [5]. At the circuit design level, we have to choose proper logic for implementing combinational circuits so that we can reduce area, power because all parameters like the choice of GDI cells, interconnects etc. are strongly influenced by the chosen logic style [1][2].

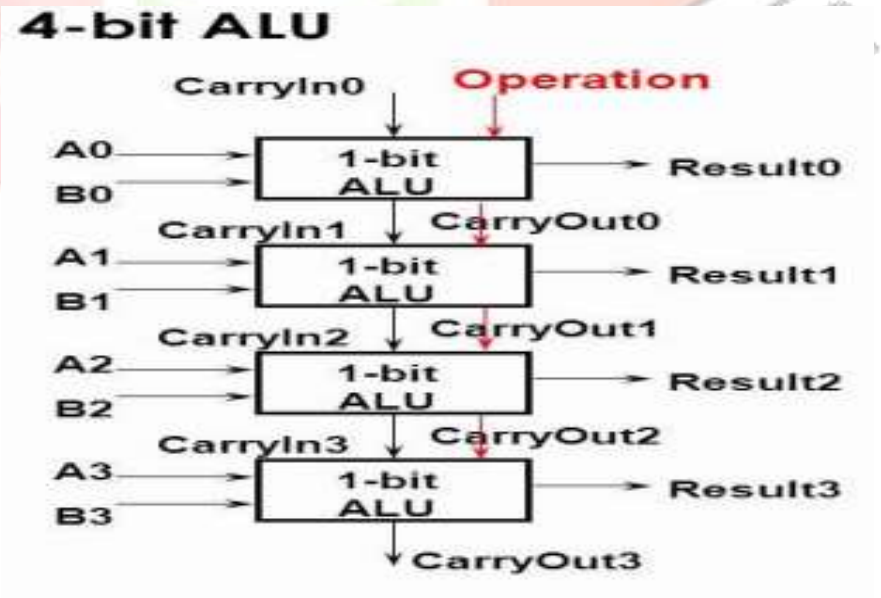

Fig. 1: basic block diagram of four bit alu

As the term arithmetic in ALU, it is used to perform an operation like addition, subtraction, multiply, divide, complement while logical includes XOR, NAND, and Multiplexer etc., and also by combining these we can make code converters and many complex combinational and sequential circuits. ALUs of various bit-widths are frequently required in very large-scale integrated circuits (VLSI) from processors to application specific integrated circuits (ASICs). Here we had designed a four-bit Arithmetic logic unit that takes take two operands (n-

bits) and give output based on the control signal. Thus; the control unit is designed by using a multiplexer which selects the required operations [4].

I.I. FEATURES OF ALU

We have designed the 4-Bit ALU which certain features as follows:

- Low-power CMOS Process Technology
- Arithmetic operations (add, subtract, complement etc.)
- Logic operations (XOR, AND, NAND, NOR, OR etc.)
- Capable of active-high and active-low operation.
- 2 selection lines are to perform the operations on two 4 bit inputs.

II. MAJOR PARTS IMPLEMENTATION AND ANALYSIS

1) **Arithmetic block:** This block is used to perform arithmetic operations such as addition, subtraction, and comparison. The core of the arithmetic block is an adder. Adders are digital circuits that carry out the addition of numbers. Adders are a key component of Arithmetic Logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BDC), Excess – 3, Gray code, Binary etc. There are two basic adders i.e. half adder and full adder.

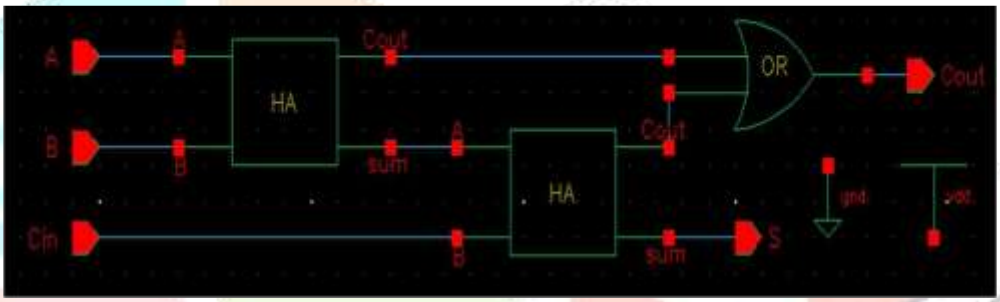

Fig. 2: semantic of full adder

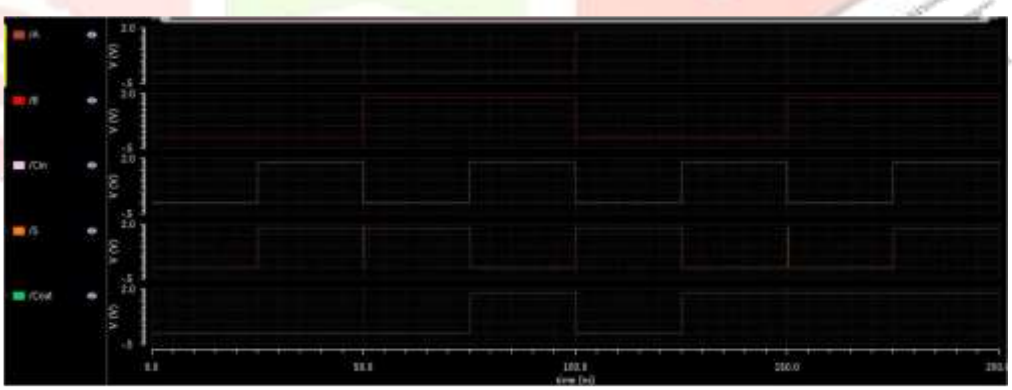

Fig. 3: waveform of full adder

2) **Logic block:** This block is used to perform simple bitwise logic operations such as AND (masking), OR and XOR, XNOR, NAND, NOT and etc.

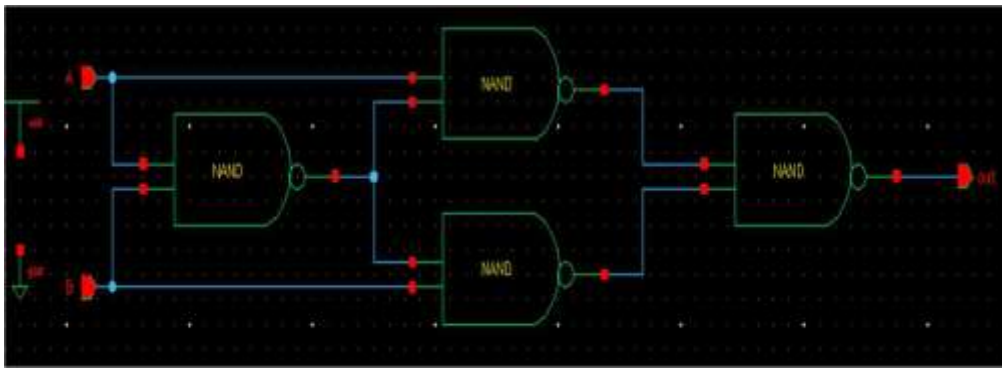

Fig. 4: semantic of xor gate

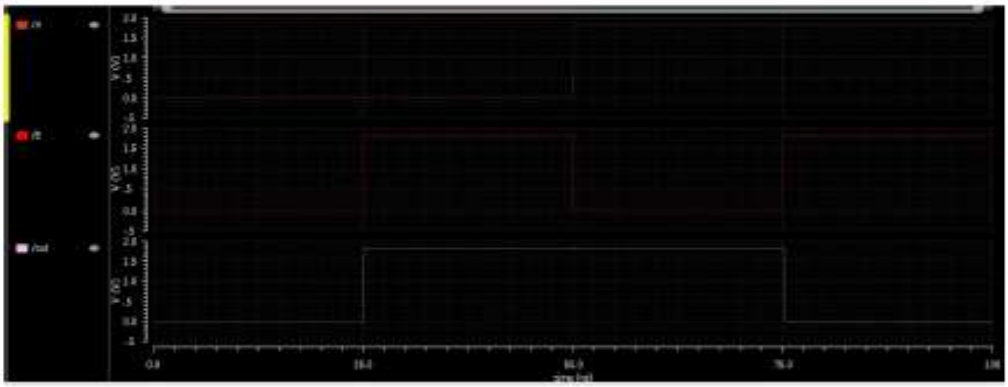

Fig. 5: waveform of xor gate

3) **Multiplexers:** A Multiplexer (or MUX) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector [3] [6].

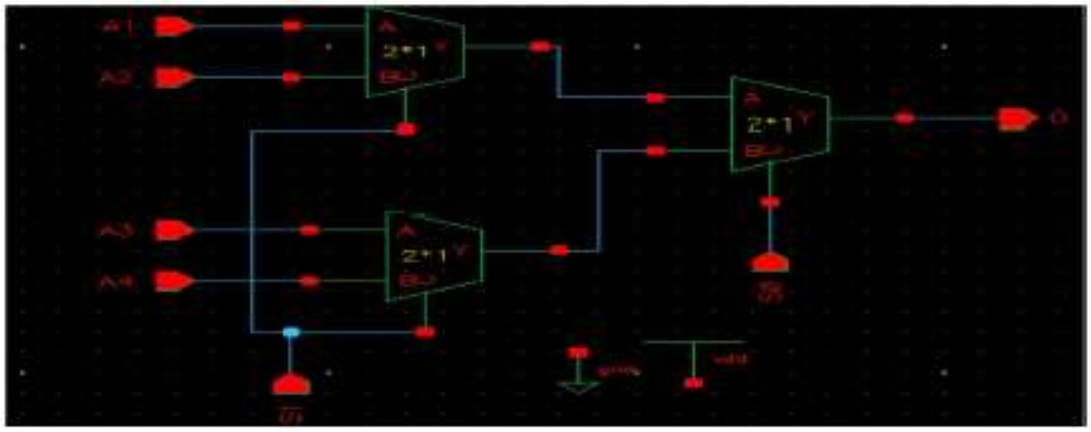

Fig. 6: semantic of 4x1 multiplexer

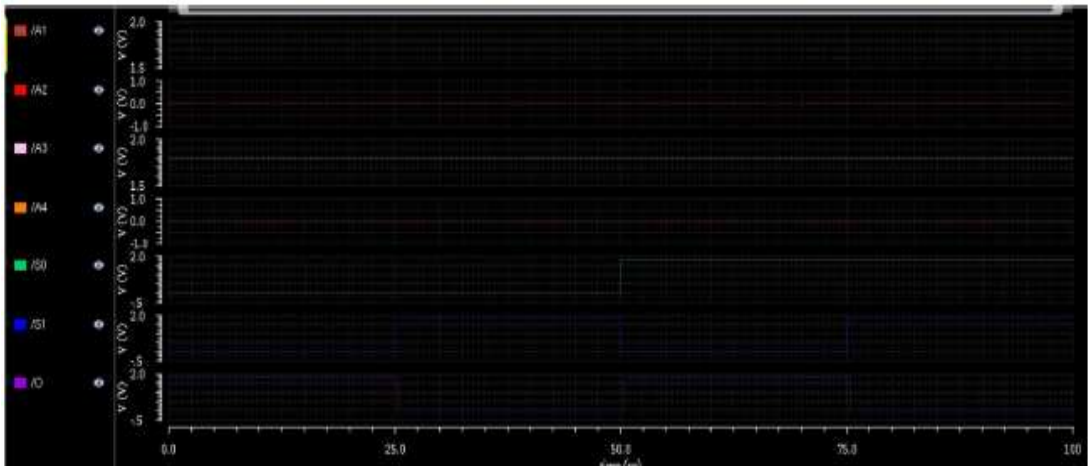

Fig. 7: waveform of 4x1 multiplexer

4) Code Converters: The availability of a large variety of codes for the same discrete elements of information results in the use of different codes by different digital systems. It is sometimes necessary to use the output of one system as the input to the other. The conversion circuit must be inserted between the two systems if each uses different codes for the same information. Thus a code converter is a circuit that makes the two systems compatible even though each uses the different code. One of the code converter is binary to gray converter which uses following basic gates which we had designed:-

$$G0 = B \oplus A \qquad G2 = D \oplus C$$

$$G1 = C \oplus B \qquad G3 = D$$

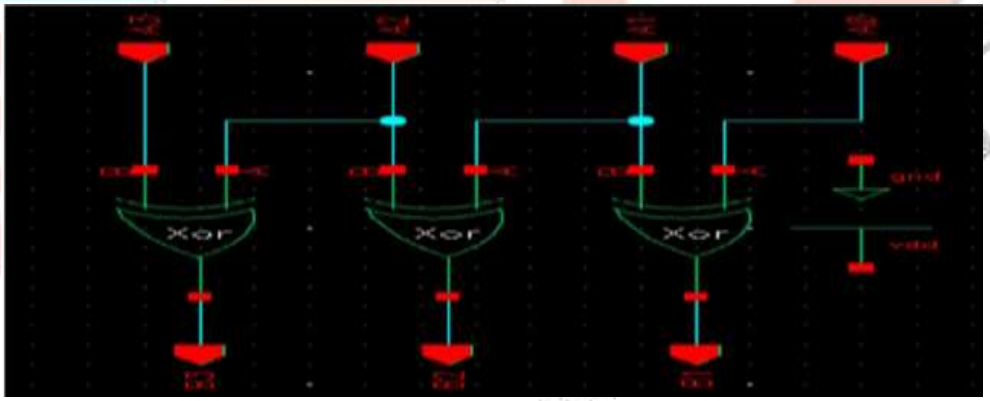

Fig. 8: semantics of binary to gray converter

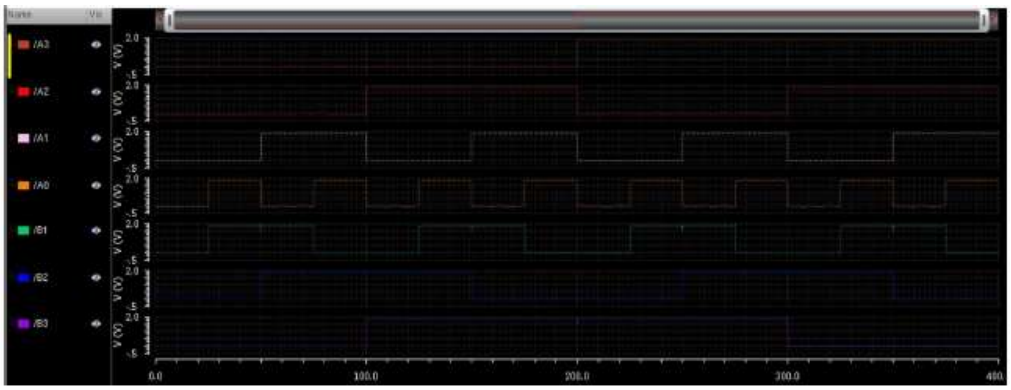

Fig. 9: waveform of binary to gray converter

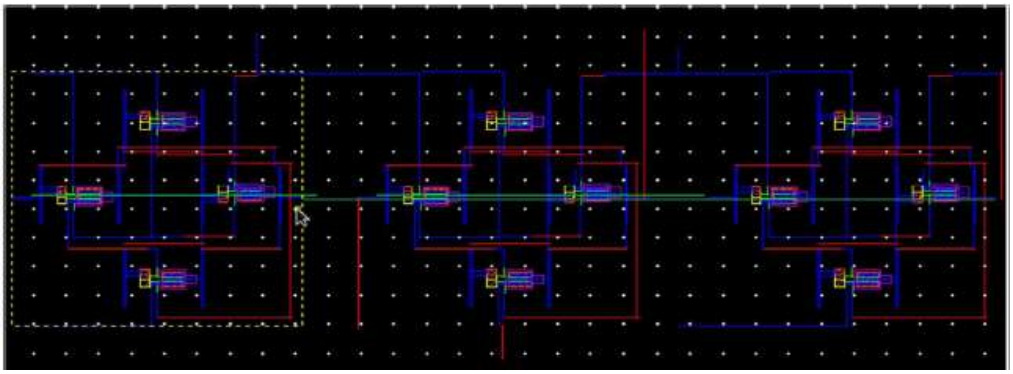

Fig. 10: layout of binary to gray converter

III. DESIGNING OF ALU USING GDI TECHNIQUE

Here we had used the virtuoso platform of cadence tool in this we design schematic of (ALU) and do the transient analysis and calculate the area and power consumption. In this design, we have used 180 nm technology. The applied voltage is 1.8V and frequency of 4.07MHz. Simulation results are obtained with better improvement in area and improvement in power consumption. ALU will perform four operations namely adder, one's complement, Binary to Gray converter and XOR depending on the selection lines selected with help of multiplexer [6] [7]. The inputs set for given result are (A0 =1 B0=0, A1= 0 B1=1, A2=1 B2=0 and A3=1 B3=1) and the simulation is

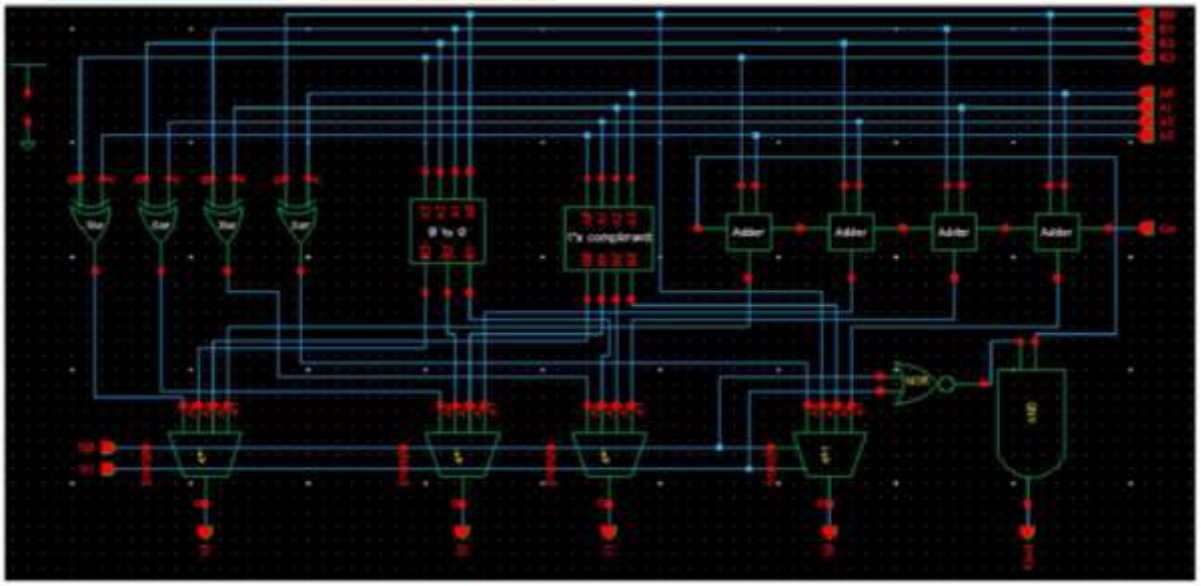

Fig. 11: semantics of arithmetic and logical unit (alu)

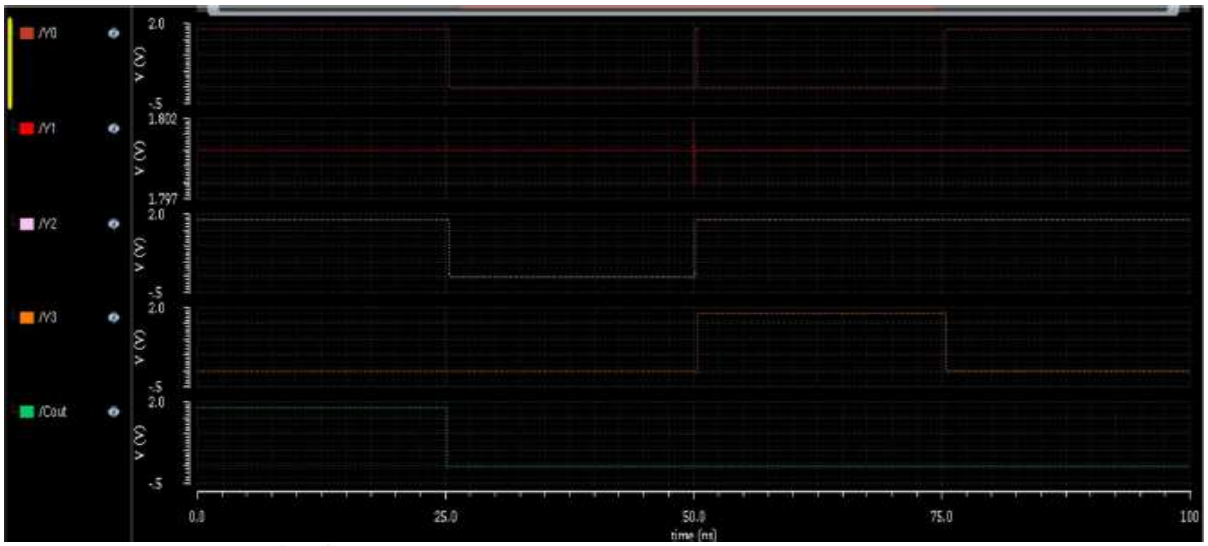

Fig. 12: waveform of arithmetic and logical unit (alu)

Table 1: mode select

TIME(ns)	S0	S1	FUNCTION
0-25	0	0	Adder
25-50	0	1	1's Compliment
50-75	1	0	Binary To Gray Converter
75-100	1	1	XOR

IV. CONCLUSION

To deal with today's competitive market, we must take a design from engineering through manufacturing with shorter design cycles and faster time to market and achieve that powerful, intuitive, and integrated tools that work seamlessly across the entire design flow are required. We have studied well about arithmetic & logic unit. Here we have implemented 4-bit arithmetic logic unit successfully. The full integrated circuit is designed and simulated in standard 180 nm CMOS technology with the aim of power and area optimization by reducing a number of transistors that leads to a minimum possible area of the circuit i.e. the reduced surface area of silicon. Proposed design proves that it has a better result in terms of performance characteristics.

V. ACKNOWLEDGEMENT

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